



Q57H-AD

V 10


SCHEMATICS TABLE:

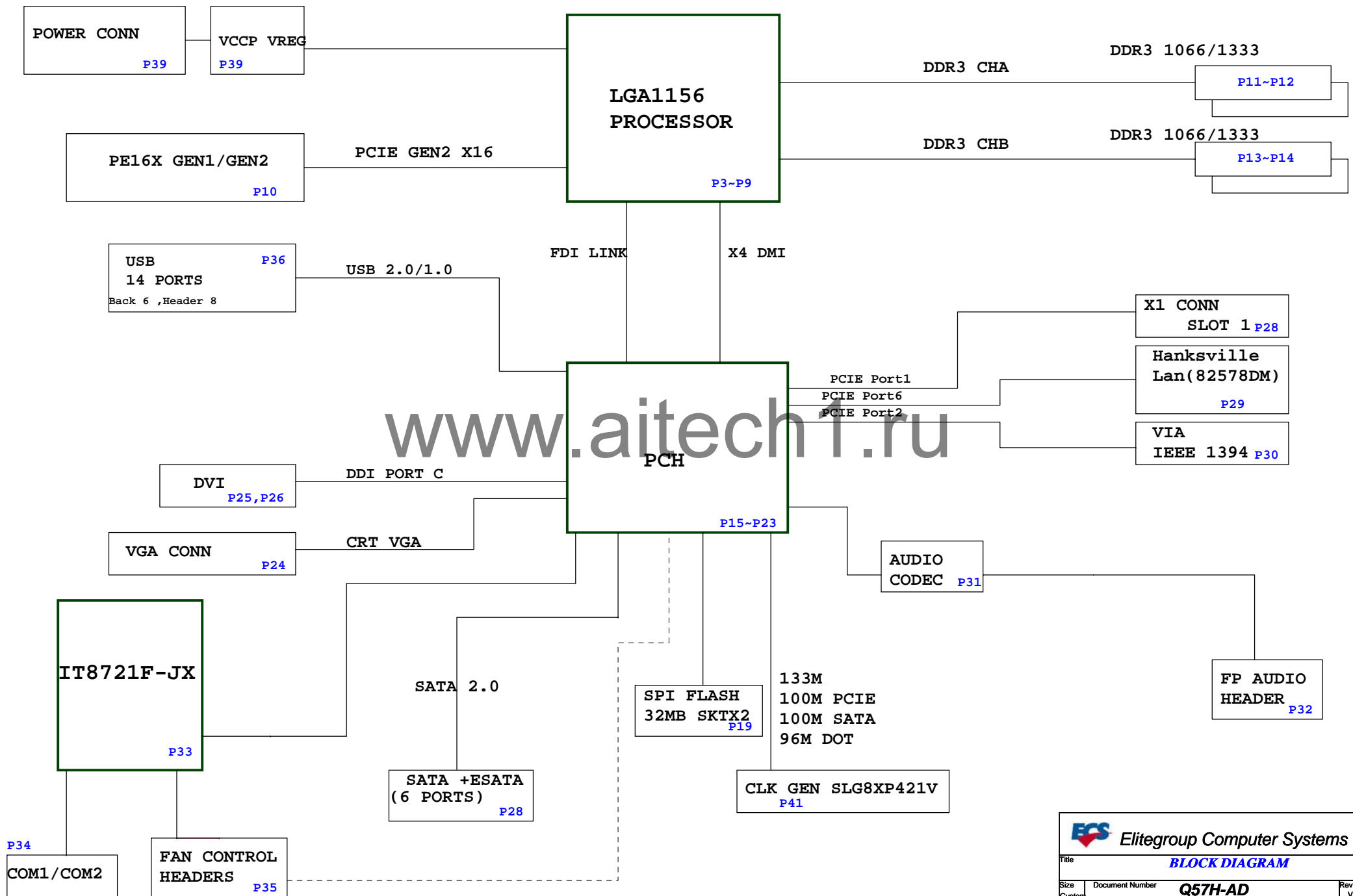
Page	Index	Page	Index
1	COVER PAGE	24	VGA Connector
2	Block Diagram	25	HDMI Interface(Shift)
3	CPU MISC&Flexible Display Interface	26	HDMI CONN
4	CPU DMI&PEG	27	Primary&PCH XDP
5	CPU DDR3-A	28	SATA&PCI-EX1
6	CPU DDR3-B	29	Hanksville Lan(82578DC)
7	CPU CFG	30	IEEE1394 (VT6315N)
8	CPU Power(VCCP,V_AXG,VTT)	31	AUDIO ALC887
9	CPU GND&RSVD	32	Audio Connector(PANEL)
10	PCI-E 16X	33	ITE 8720F/ITE 8721
11	CONN DDR3 CH A DIMM2	34	COM,KBMS,FDD,LPT
12	CONN DDR3 CH A DIMM1	35	PANEL&Smart Fan
13	CONN DDR3 CH B DIMM4	36	USB Header&Port
14	CONN DDR3 CH B DIMM3	37	DC-DC3 CPU_VTT,5VDUAL
15	PCH USB&PCIE&DMI	38	DC-DC2 V_AXG,V_1P05_ME
16	PCH SATA,HOST,CLINK,PCI	39	DC-DC4 PCH Core,VDIMM,V_1P8
17	PCH GPIO,AUDIO,LPC,SPI,BAT	40	DC-DC Vcore
18	PCH NVRAM	41	CLK GEN SLG8XP421V
19	PCH FDLINK&SPI ROM&TPM	42	EUP LOT6
20	PCH PWR RAILS,Decoupling	43	POWER DELIVERY
21	PCH GND Pins	44	PWRGD AND RST Tree
22	PCH Video and DDSP	45	Clock Map
23	PCH CLOCKS,Straps		

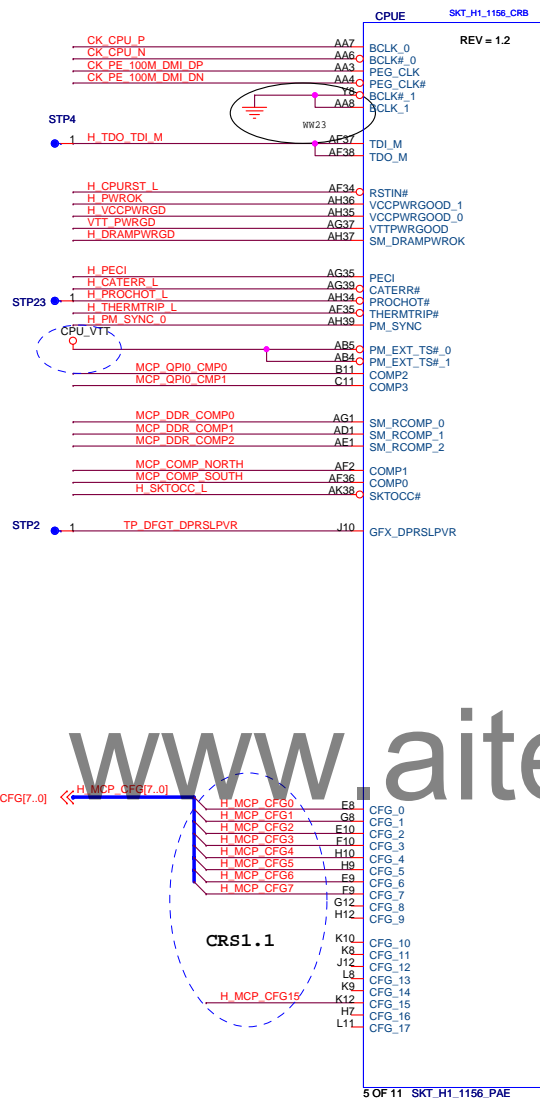
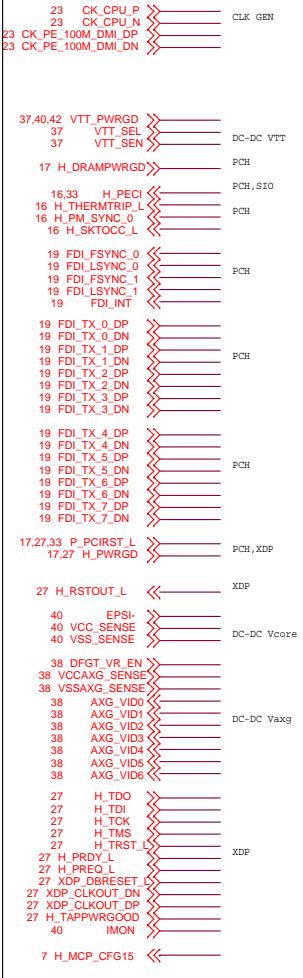
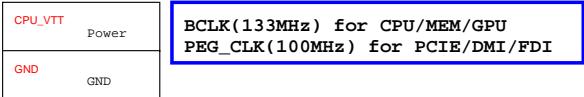
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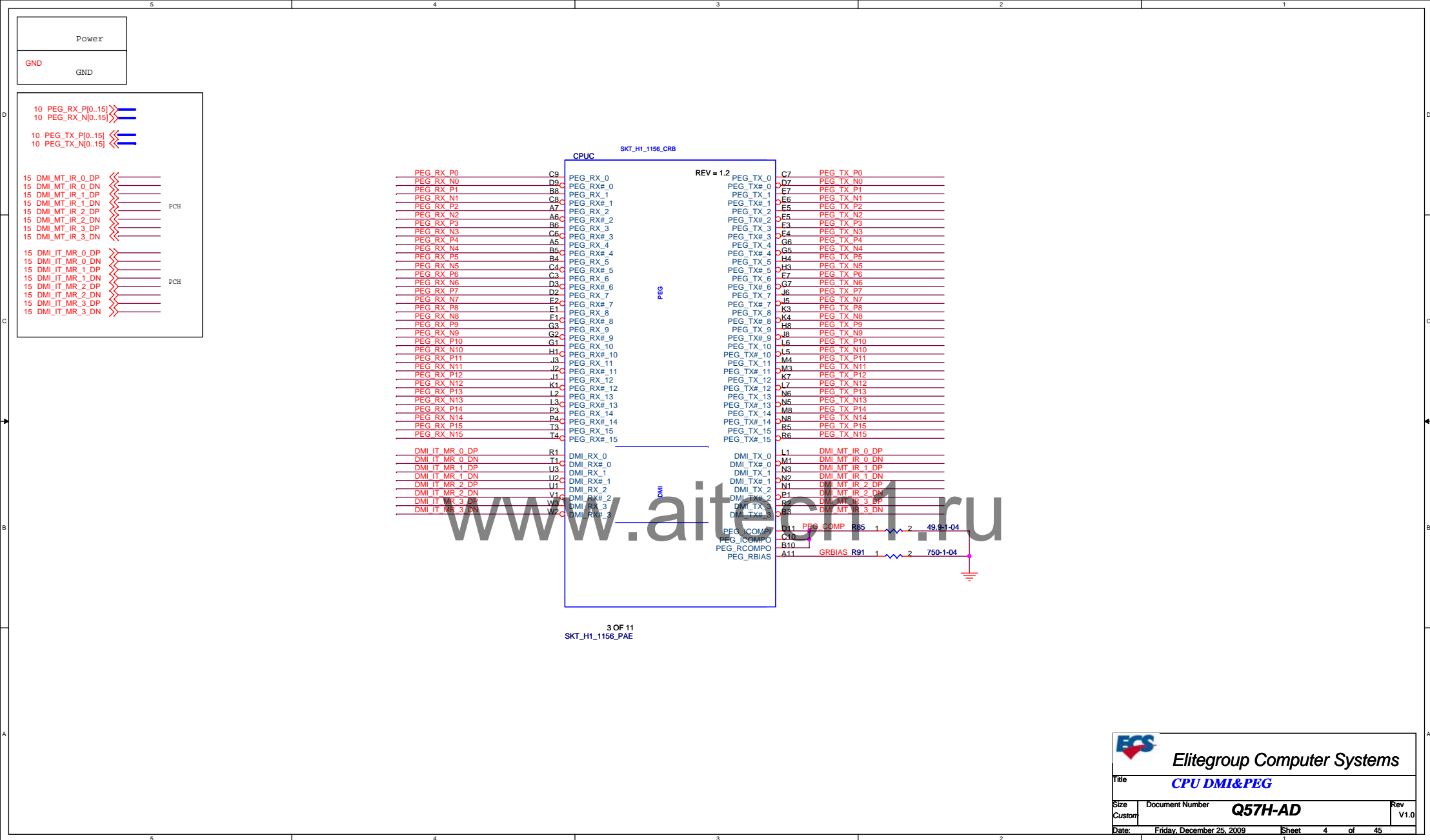
Rev	Date	Notes
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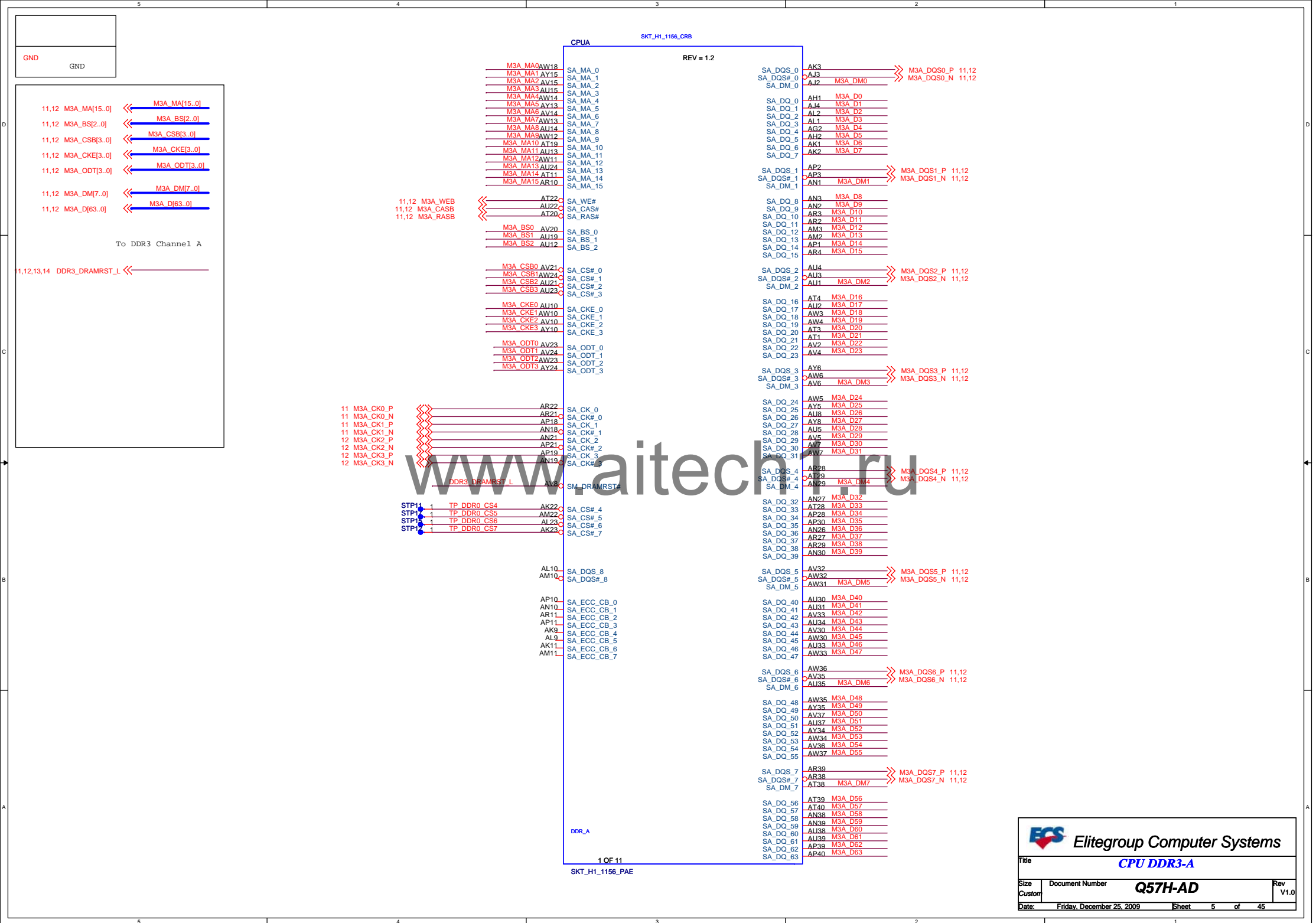
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CONFIDENTIAL @

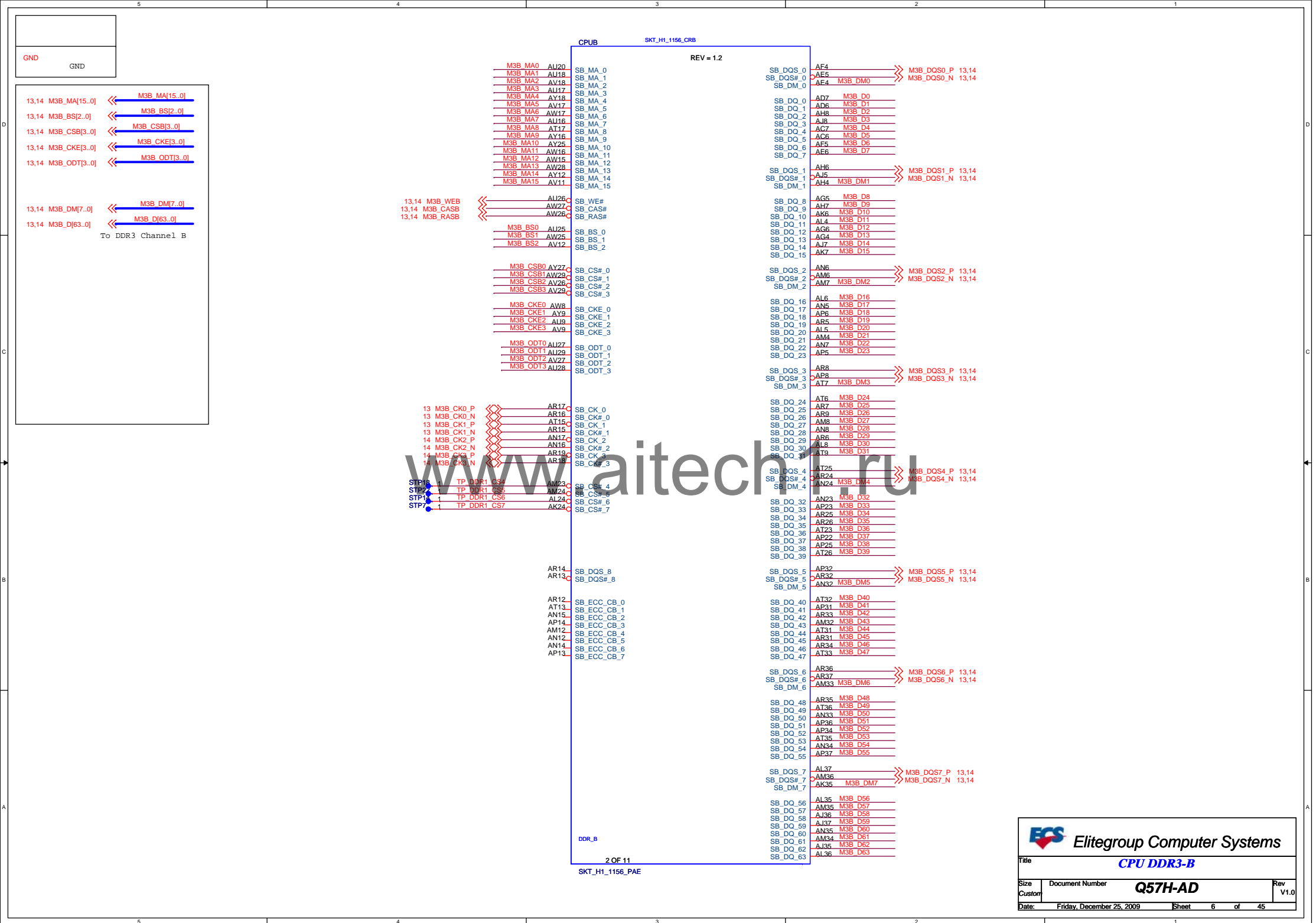
 Elitegroup Computer Systems	
Title Cover Page	
Size Custom	Document Number Q57H-AD Rev V10
Date: Friday, December 25, 2009	Sheet 1 of 45

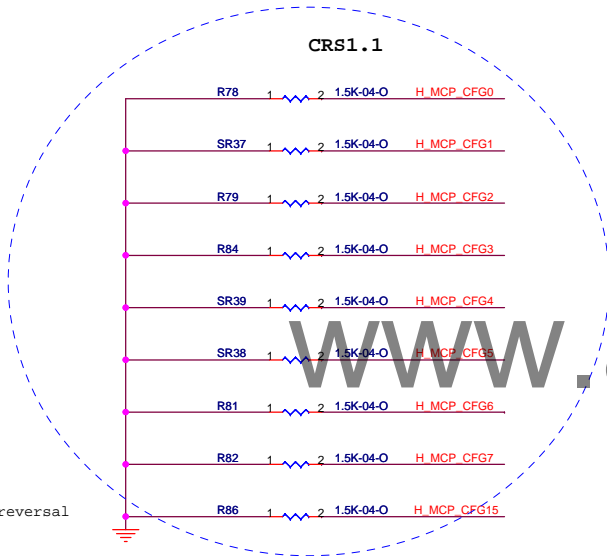
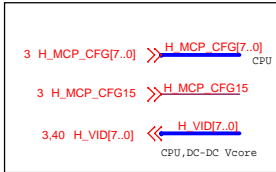
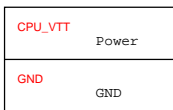






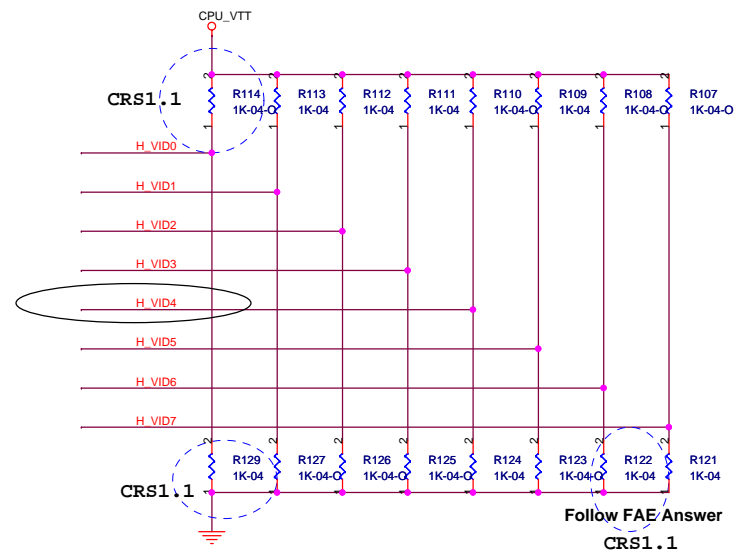






CFG(1:0)
Desktop
11 PCIE16X
10 PCIE18X
CFG2,4,5,6,7~17
Reserved configuration land
CFG3
Havendale PCIE static Lan Numbering reversal

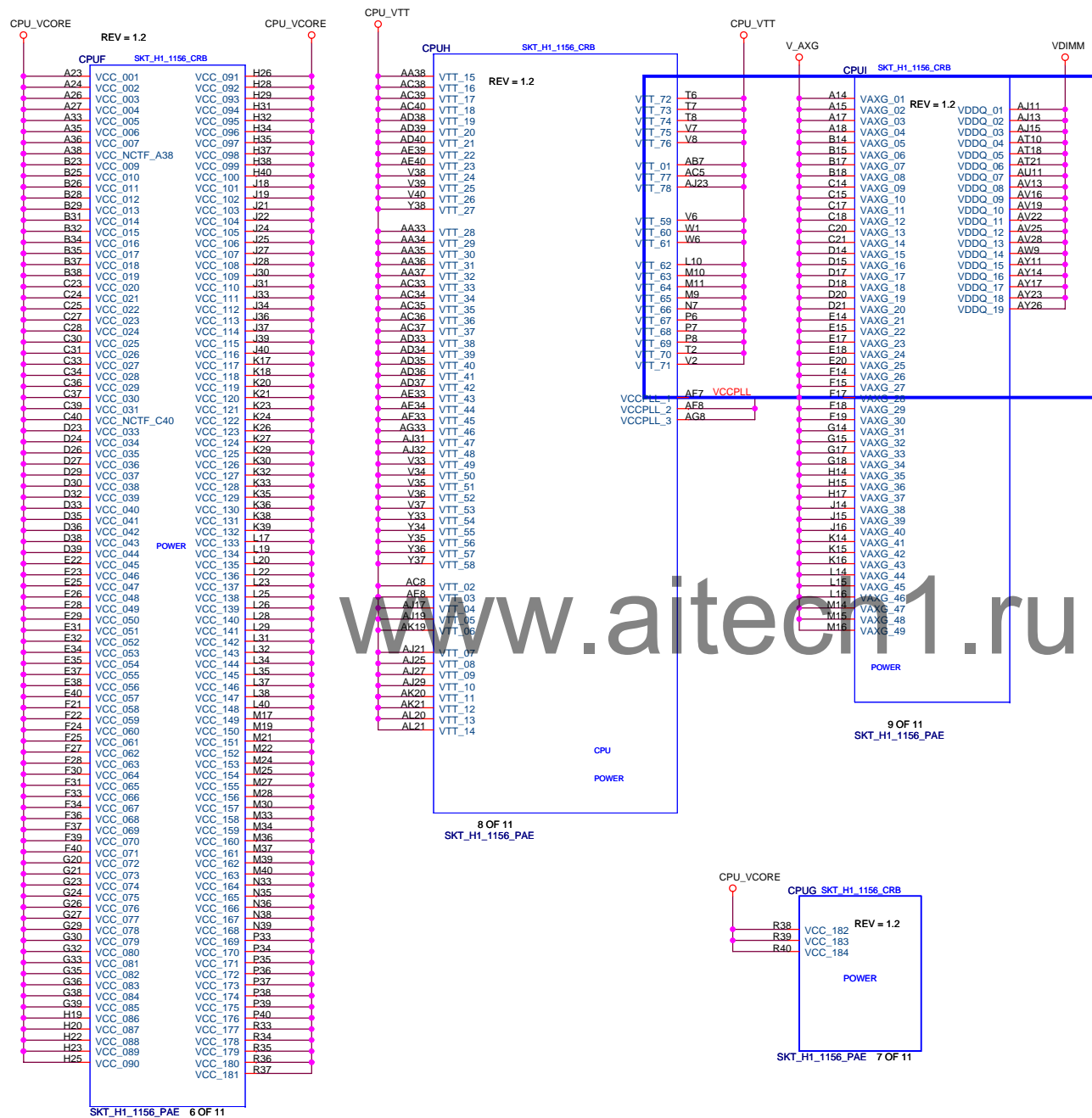
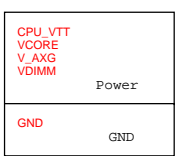
CFG	Havendale	Lynnfield			
		1	11=1*16X	0	10=2*8X
0	REVERSED	1		0	
1	REVERSED	1		1	
2	REVERSED			REVERSED	
3	Static Lane Number Reversal			REVERSED	
4	REVERSED			REVERSED	
6	REVERSED				
7	REVERSED				
15	REVERSED				
0,1,2,3,4,5 ALL HAVE INTERNAL PULL-UPS					

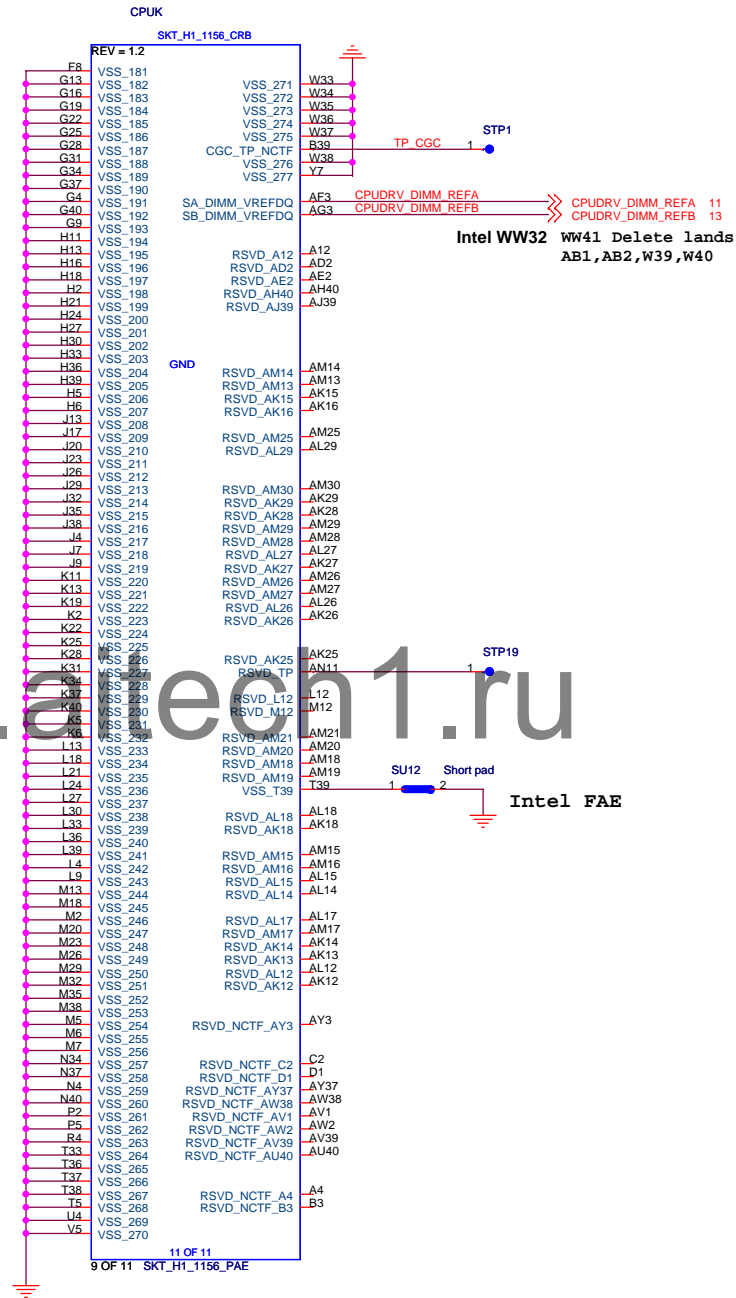
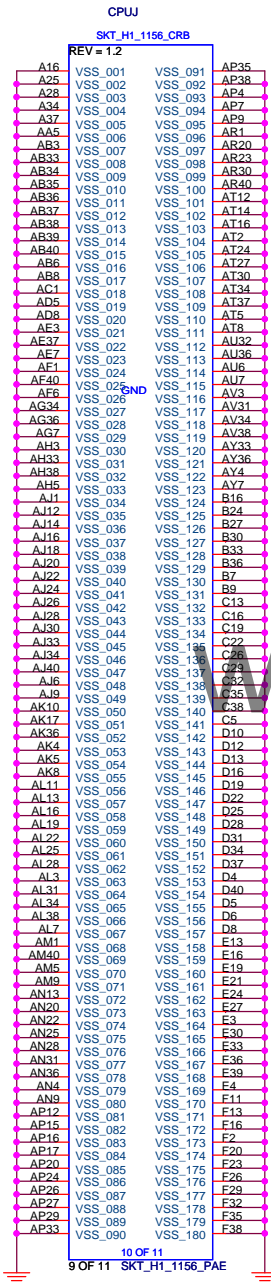
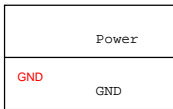


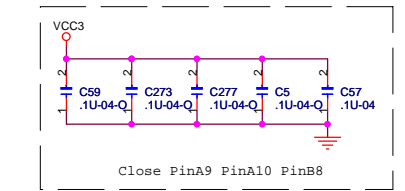
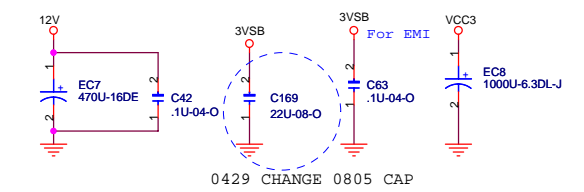
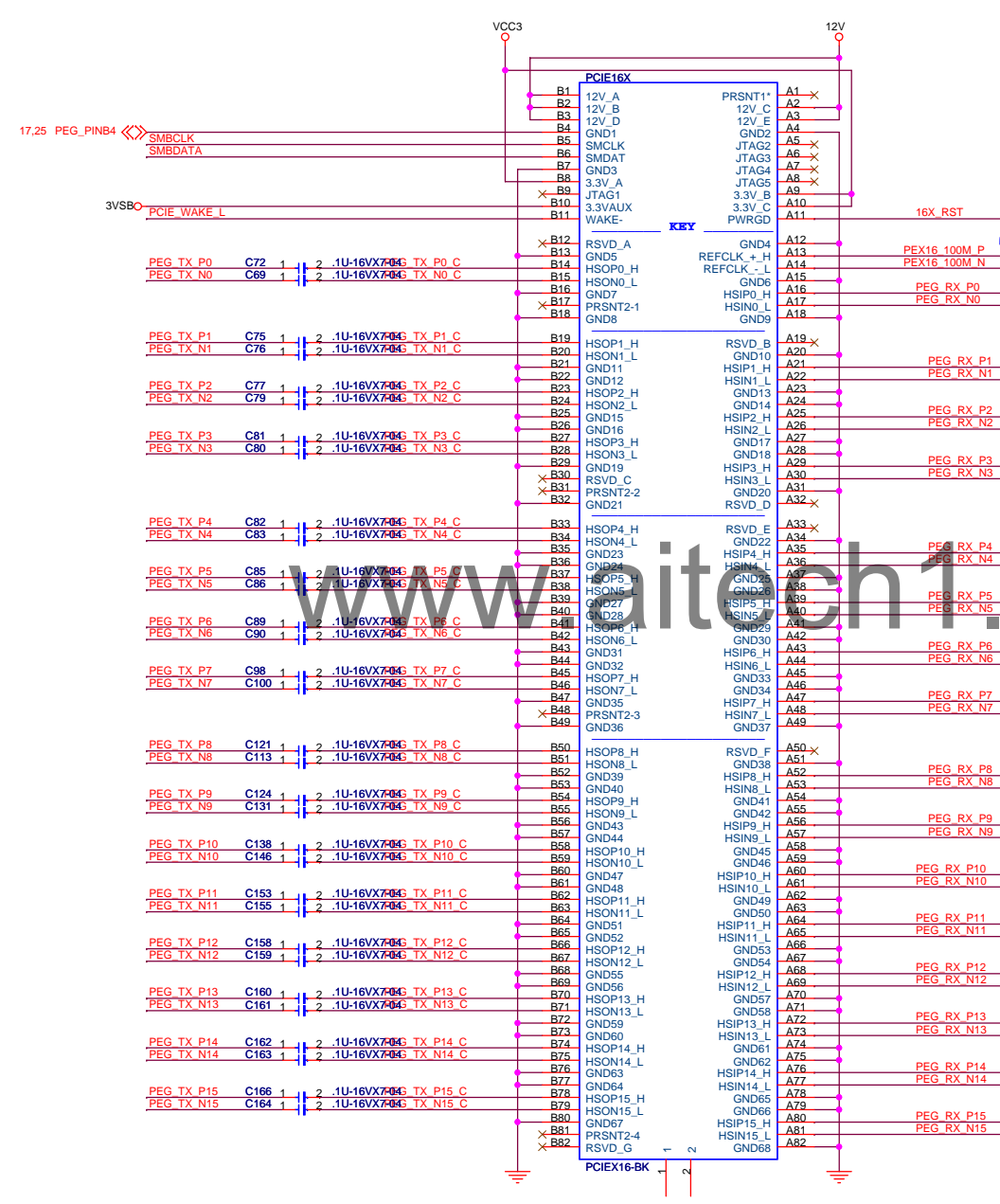
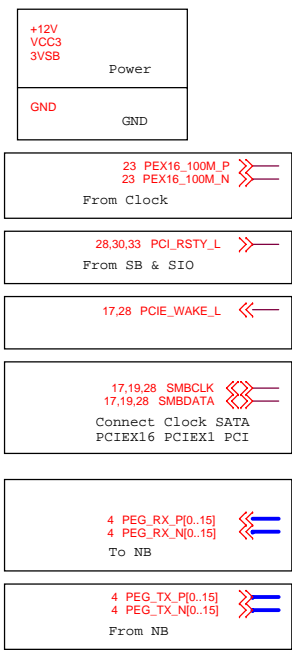
POWER ON CONFIGURATION (POC)TABLE

	FUNCTION	Setting	Havendale	Lynnfield
VID0	MIS0	0	Support	Support
VID1	MIS1	1		
VID2	MIS2	1		
VID3	IMON CONFIG CSC0	1	Icc(MAX)=120A	Icc(MAX)=120A
VID4	IMON CONFIG CSC1	0		
VID5	IMON CONFIG CSC2	1		
VID6	RESERVED	0		
VID7	VID SELECT	0		
PSI#	RESERVED	LOW		

*MSID(2:0)
110 Lynnfield and Havendale support
*CSC(0:2)
Iout Gain and POC setting
100 ICC(max) 80A~100A
101 ICC(max) 100A~120A
110 ICC(max) 120A~140A

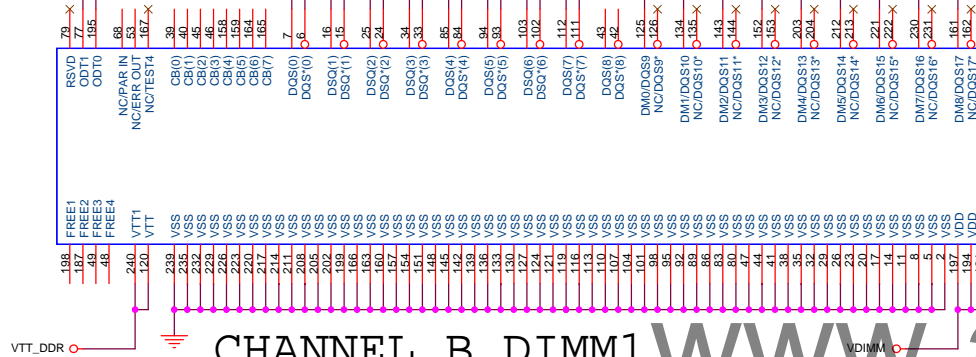






6.13 M3B_DQS7_N
6.13 M3B_DQS7_P
6.13 M3B_DQS6_N
6.13 M3B_DQS6_P
6.13 M3B_DQS5_N
6.13 M3B_DQS5_P
6.13 M3B_DQS4_N
6.13 M3B_DQS4_P
6.13 M3B_DQS3_N
6.13 M3B_DQS3_P
6.13 M3B_DQS2_N
6.13 M3B_DQS2_P
6.13 M3B_DQS1_N
6.13 M3B_DQS1_P
6.13 M3B_DQS0_N
6.13 M3B_DQS0_P

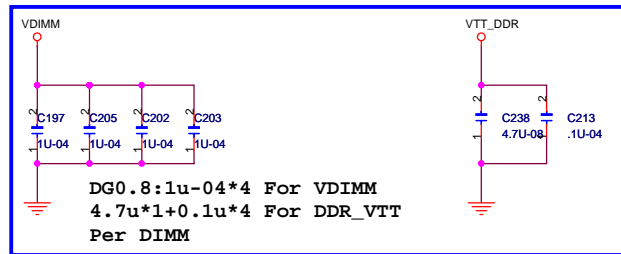
M3B_ODT2
M3B_ODT3



CHANNEL B DIMM1

13 DIMM_CA_VREF_B
13 DIMM_DQ_VREF_B
11,12,13,19,27,41 SCLK
11,12,13,19,27,41 SDATA

DIMM CA_VREF_B
DIMM DQ_VREF_B
SCLK
SDATA



DG0.8:1u-04*4 For VDIMM
4.7u*1+0.1u*4 For DDR_VTT
Per DIMM

DDR_VTT	Power
VDIMM	
DIMM_VDDSPD	
GND	GND

6.13 M3B_D[63..0]

6.13 M3B_DM[7..0]

6.13 M3B_MA[15..0]

6.13 M3B_ODT[3..0]

6.13 M3B_CS[3..0]

6.13 M3B_CKE[3..0]

6.13 M3B_BS[2..0]

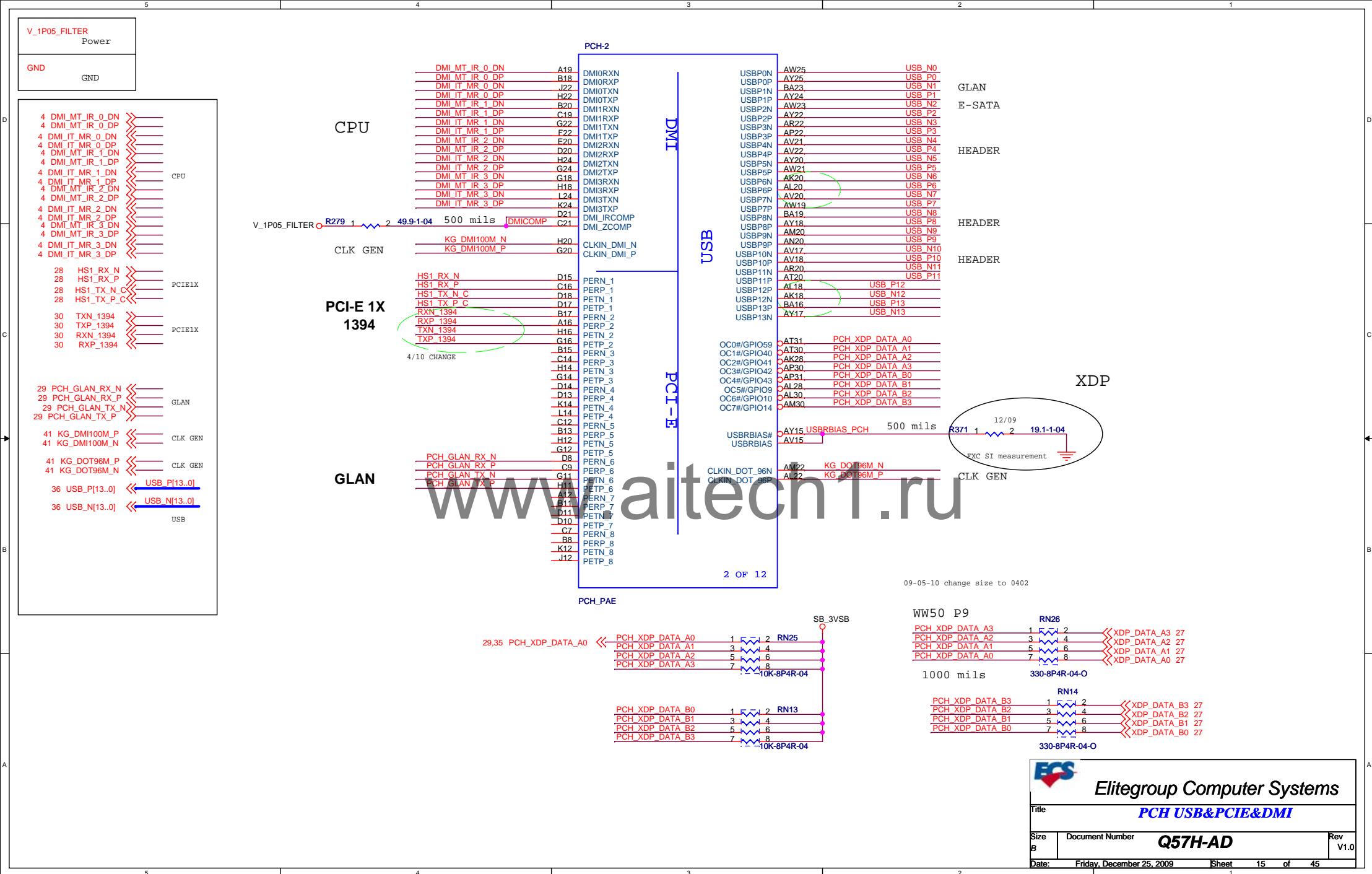
DIMM3

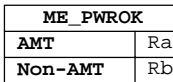
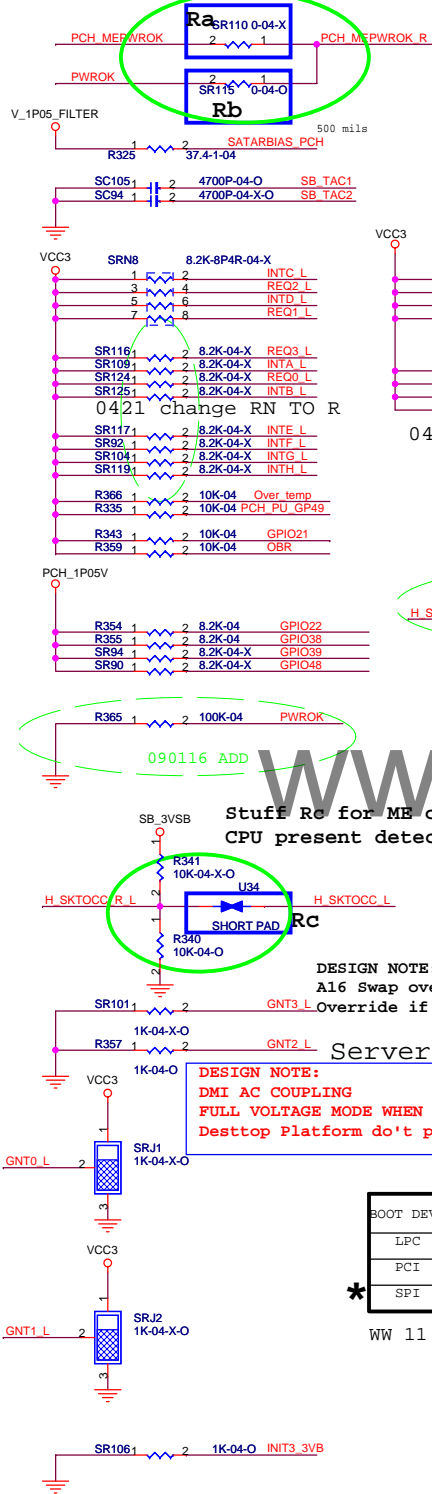
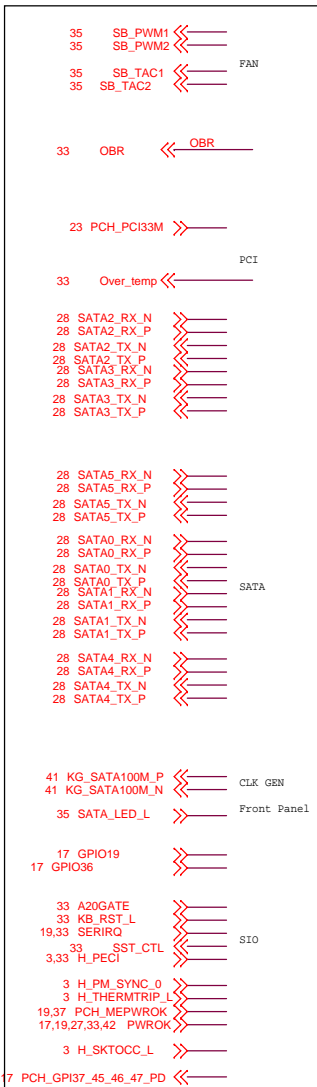
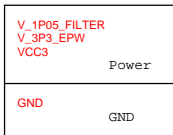
DDR3-240P-GR

M3B_WEB
M3B_RASB
M3B_CASB

DDR3_DRAMRST_L 5,11,12,13

M3B_CK2_P 6
M3B_CK2_N 6
M3B_CK3_P 6
M3B_CK3_N 6





DESIGN NOTE:
Al6 Swap override
Override if sampled low

Server Only

DESIGN NOTE:
DMI AC COUPLING
FULL VOLTAGE MODE WHEN SAMPLED LOW
Desktop Platform do't pull low

BOOT DEVICE	GNT1	GNT0
LPC	0	0
PCI	1	0
SPI	1	1

WW 11 PCI CHANGE TO 10

FAN

NOT USE

SST CTL

SC99

220PF-04-X-O

AN41

GPIO22

GPIO38

GPIO39

GPIO48

AN31

SCLOCK/GPIO22

SLOAD/GPIO38

SDATAOUT0/GPIO39

SDATAOUT1/GPIO48

AF15

NC_AF15

AG37

A20GATE

INIT3_3VB

RCIN#

AM40

KB_RST_L

AL40

SERIRQ

C38

H_THERMTRIP_L

D36

R277

H_P_M_SYNC_0

H_PECI

C37

USE SIO_FAN RESERVE

0504 del PAR-PME-PCIRST

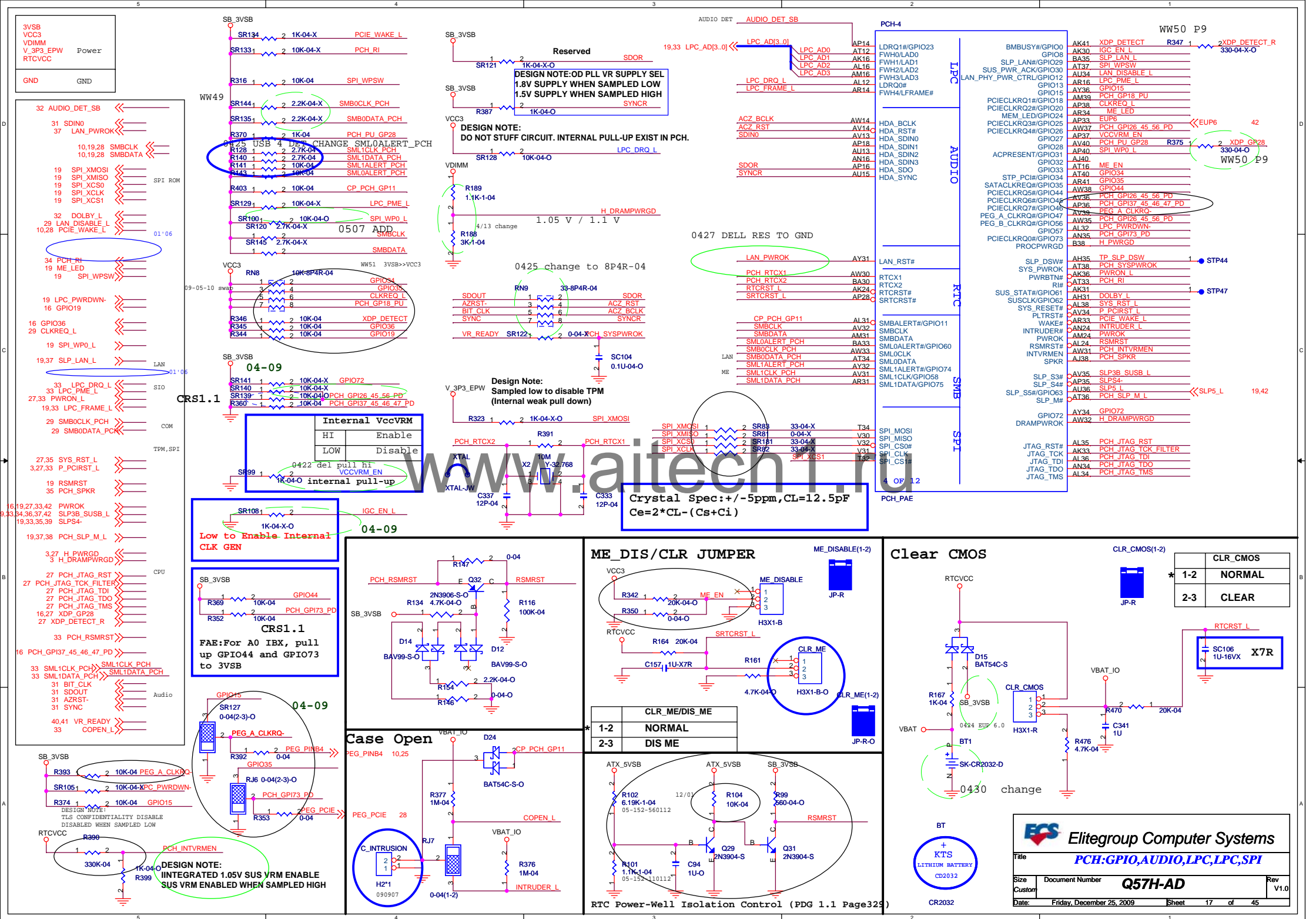
DEVSEL_L

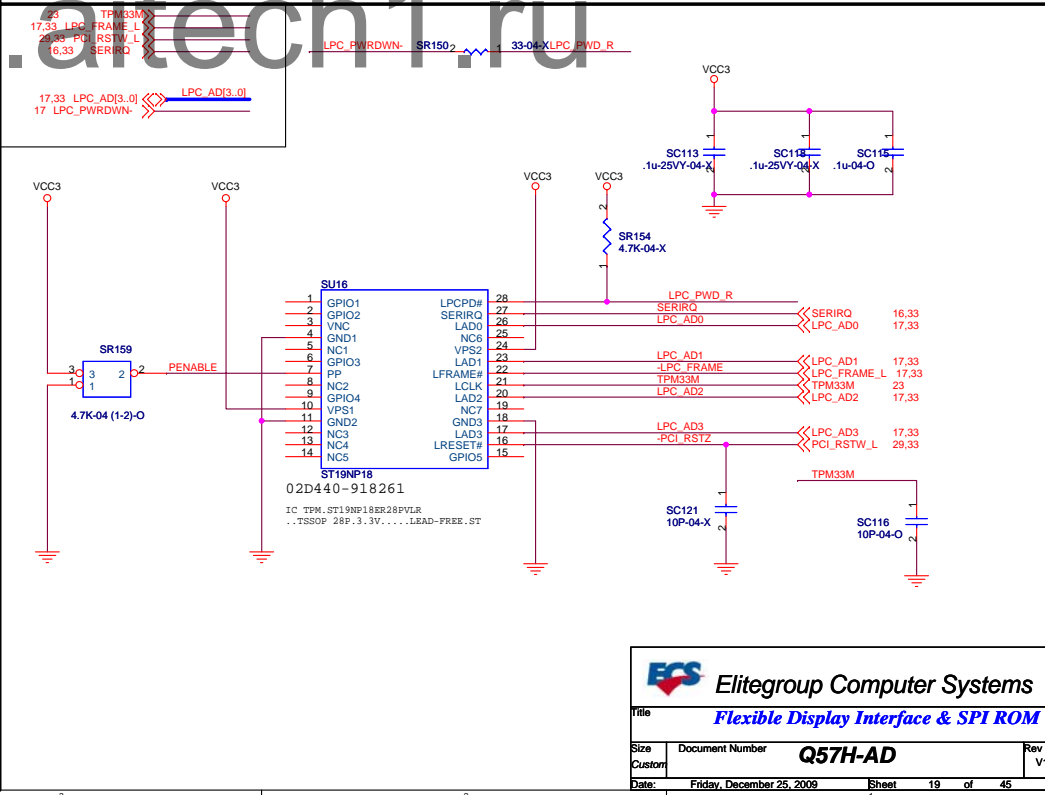
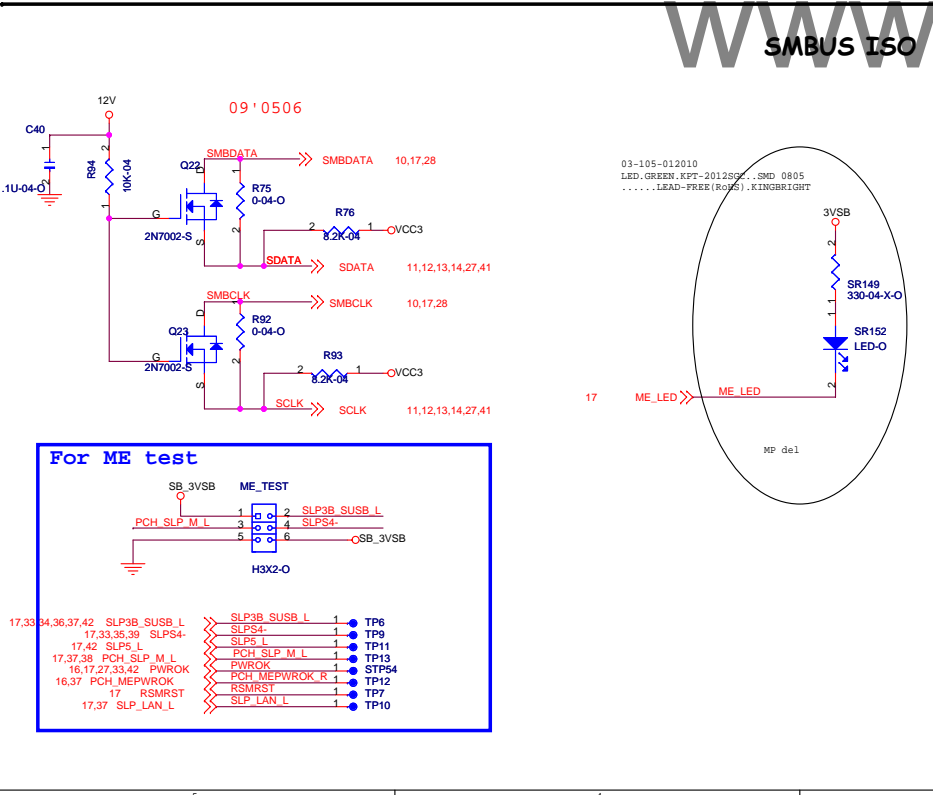
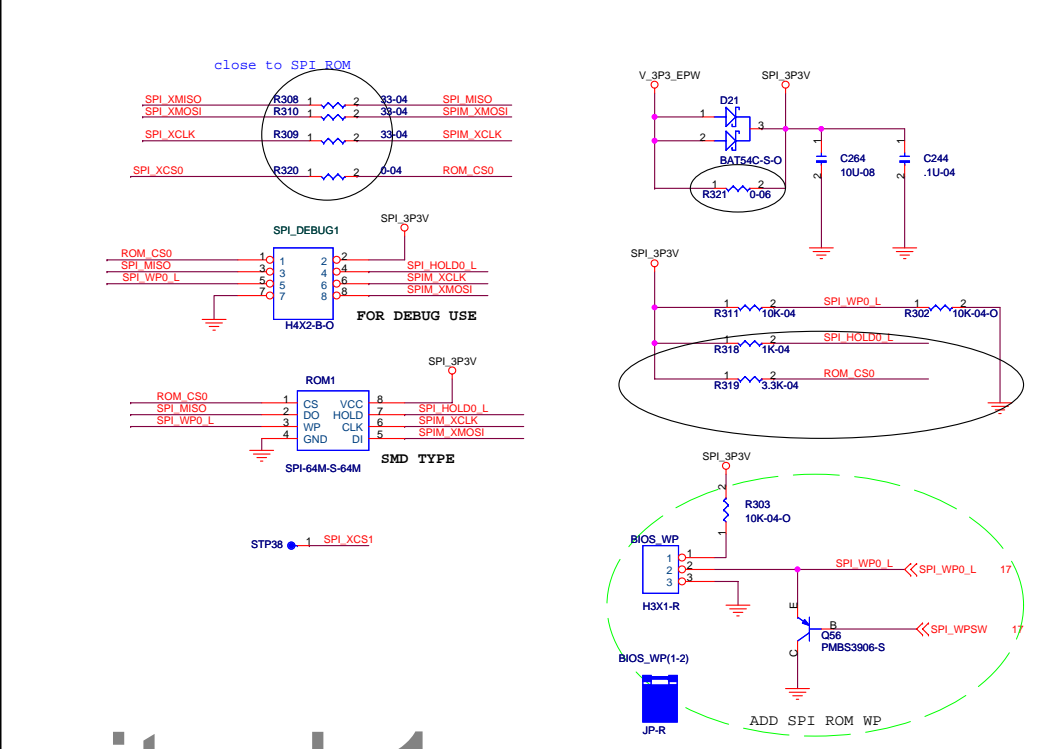
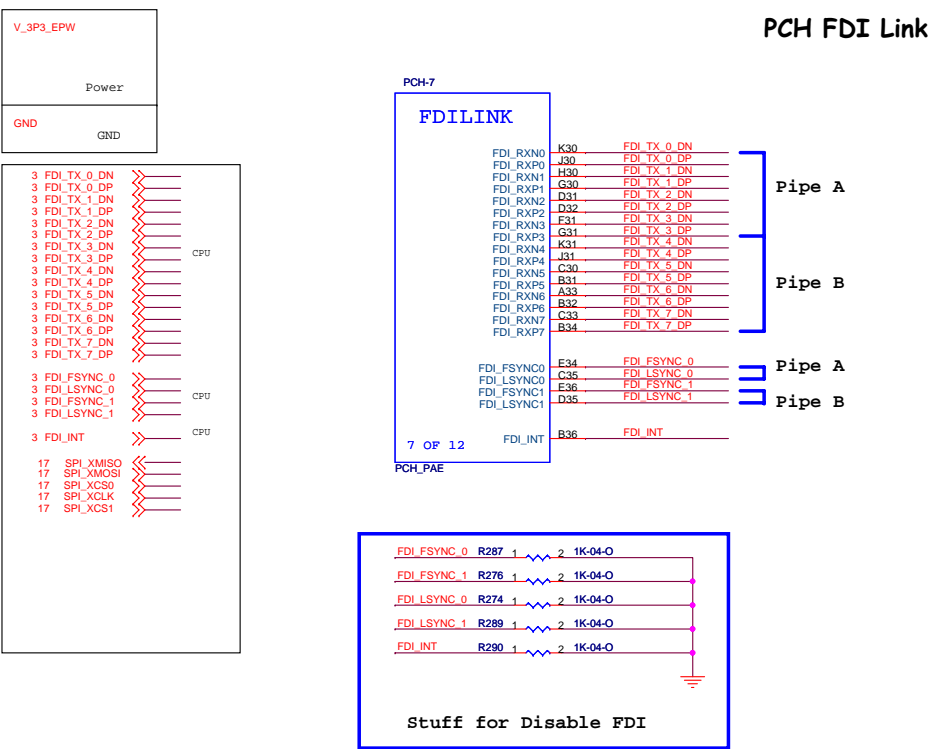
AT6

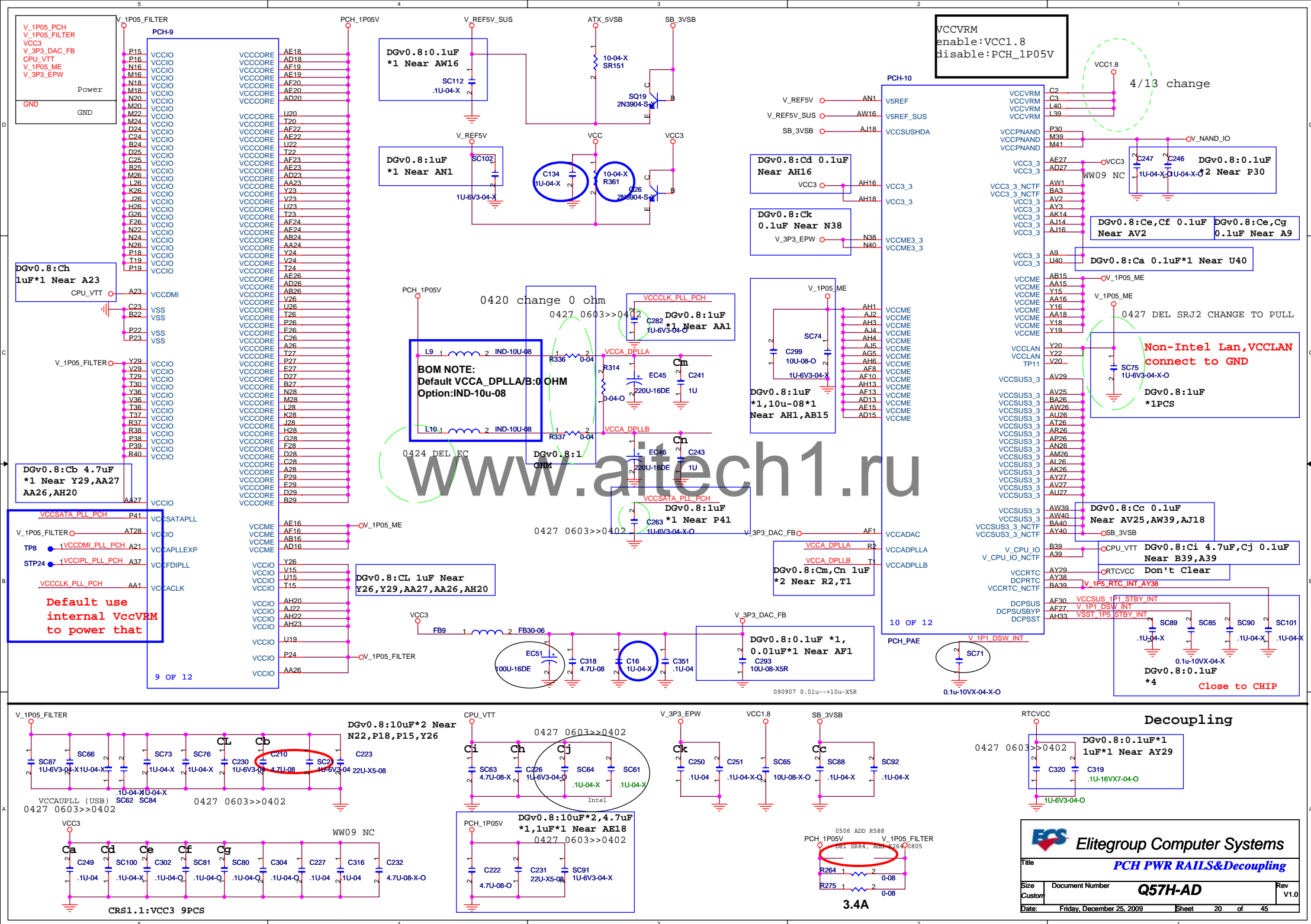
PCH_PCI33M

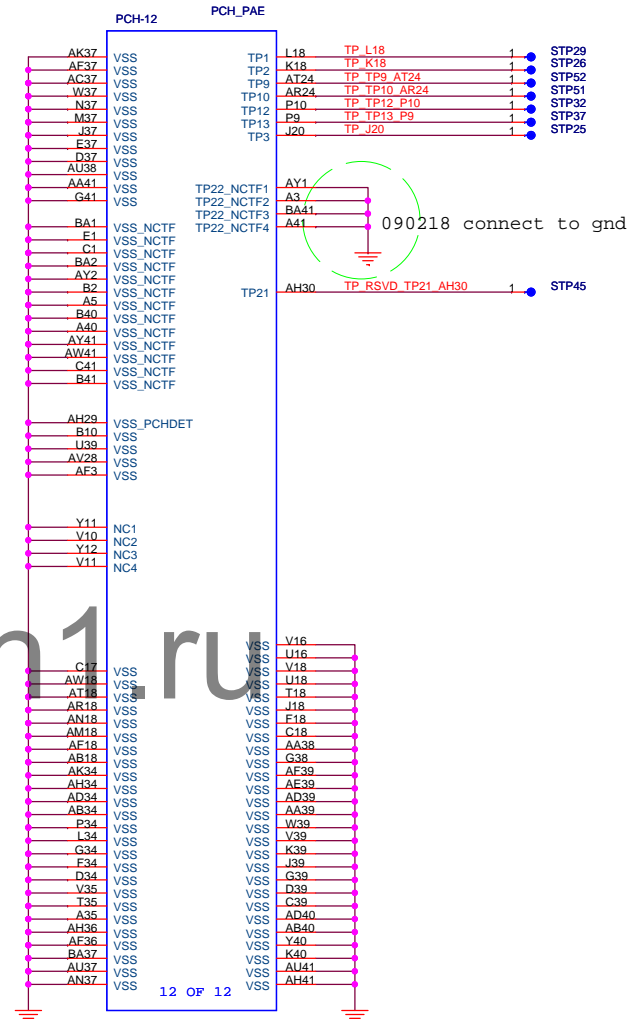
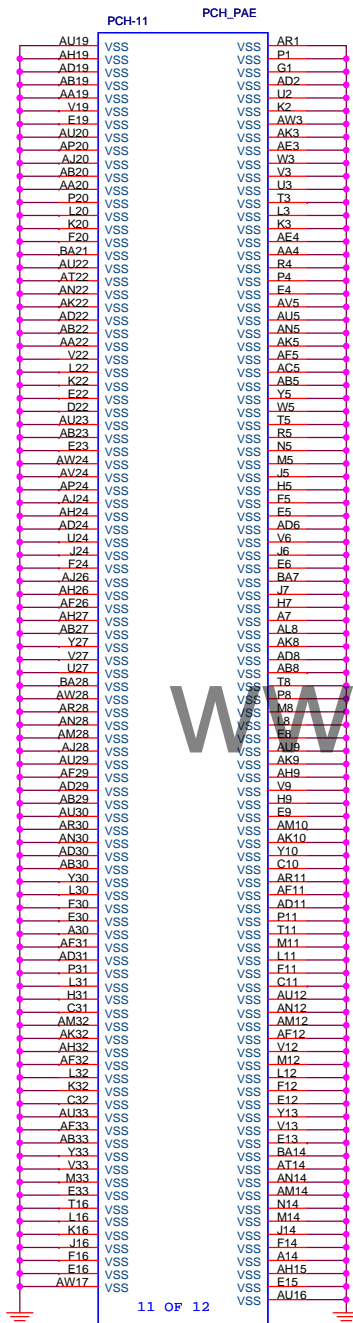
AL11

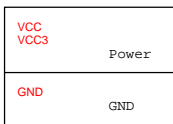
 IRDY# | PCIRST# || IRDY# | PCIRST# |
SERR_L	PME#
STOP_L	SERR#
PLOCK_L	STOP#
TRDY_L	PLOCK#
PERR_L	TRDY#
FRAME_L	PERR#
FRAME_L	FRAME#
GNT0_L	AK11
GNT1_L	AK6
GNT2_L	BA9
GNT3_L	AM3
REQ0_L	AP4
REQ1_L	AW5
REQ2_L	AY4
REQ3_L	AH8
INTA_L	AT8
INTB_L	AR4
INTC_L	AT11
INTD_L	BA5
INTE_L	AL6
INTF_L	AH7
INTG_L	AP12
INTH_L	AW4
INTI_L	PIROA#
INTJ_L	PIROB#
INTK_L	PIROC#
INTL_L	PIROD#
INTM_L	PIROE#
INTN_L	PIROF#
INTO_L	PIROG#
INTP_L	PIROH#
INTQ_L	PIROI#
INTR_L	PIROJ#
INTS_L	PIROK#
INTT_L	PIROL#
INTU_L	PIROM#
INTV_L	PIRON#
INTW_L	PIROO#
INTX_L	PIROP#
INTY_L	PIROQ#
INTZ_L	PIROS#
INTAA_L	PIROT#
INTAB_L	PIROU#
INTAC_L	PIROV#
INTAD_L	PIROW#
INTAE_L	PIROX#
INTAF_L	PIROY#
INTAG_L	PIROZ#
INTAH_L	PIROA#
INTAI_L	PIROB#
INTAJ_L	PIROC#
INTAK_L	PIROD#
INTAL_L	PIROE#
INTAM_L	PIROF#
INTAN_L	PIROG#
INTAO_L	PIROH#
INTAP_L	PIROI#
INTAQ_L	PIROJ#
INTAR_L	PIROK#
INTAS_L	PIROL#
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INTAW_L	PIROP#
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INTBD_L	PIROX#
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INTBP_L	PIROJ#
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INTBS_L	PIROM#
INTBT_L	PIRON#
INTBU_L	PIROO#
INTBV_L	PIROP#
INTBW_L	PIROQ#
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INTBY_L	PIROT#
INTBZ_L	PIROU#
INTCA_L	PIROV#
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INTCV_L	PIROO#
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INTHU_L	PIROO#
INTHV_L	PIROP#
INTHW_L	PIROQ#
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INTHY_L	PIROT#
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INTIU_L	PIROO#
INTIV_L	PIROP#
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INTIY_L	PIROT#
INTIZ_L	PIROU#
INTJA_L	PIROV#
INTJB_L	PIROW#
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INTJH_L	PIROB#
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INTJS_L	PIROM#
INTJT_L	PIRON#
INTJU_L	PIROO#
INTJV_L	PIROP#
INTJW_L	PIROQ#
INTJX_L	PIROS#
INTJY_L	PIROT#
INTJZ_L	PIROU#
INTKA_L	PIROV#
INTKB_L	PIROW#
INTKC_L	PIROX#
INTKD_L	PIROY#
INTKE_L	PIROZ#
INTKf_L	PIROA#
INTKH_L	PIROB#
INTKI_L	PIROC#
INTKJ_L	PIROD#
INTKK_L	PIROE#
INTKL_L	PIROF#
INTKM_L	PIROG#
INTKN_L	PIROH#
INTKO_L	PIROI#
INTKP_L	PIROJ#
INTKQ_L	PIROK#
INTKR_L	PIROL#
INTKS_L	PIROM#
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INTQA_L	PI





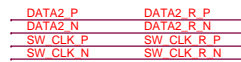
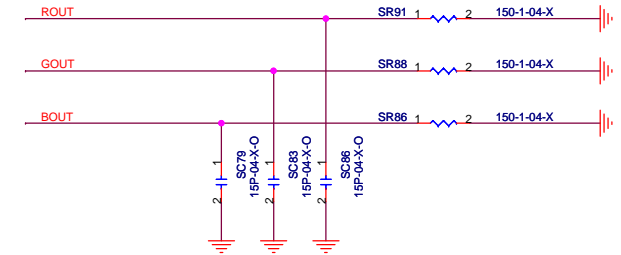
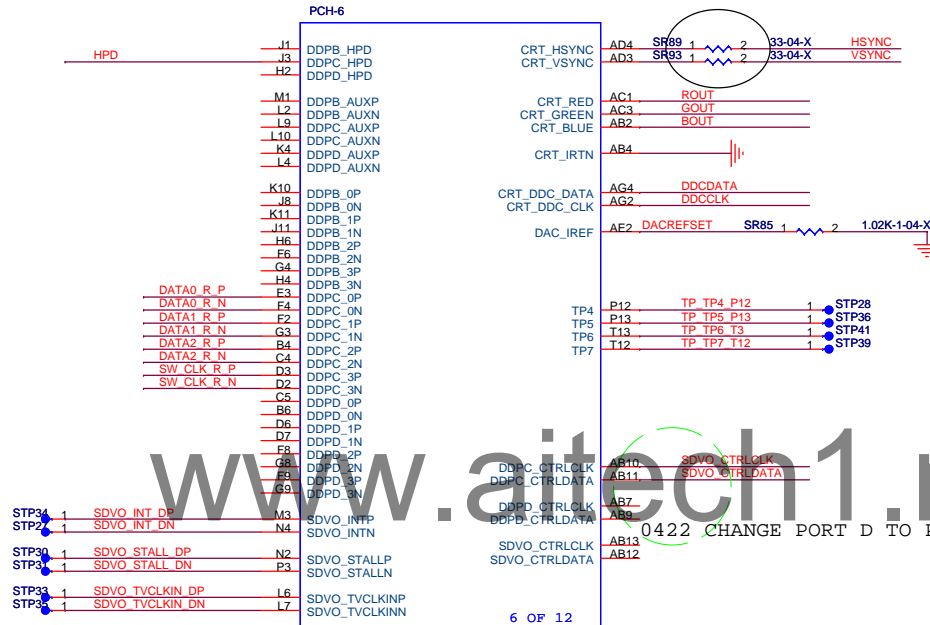
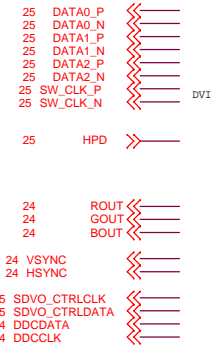


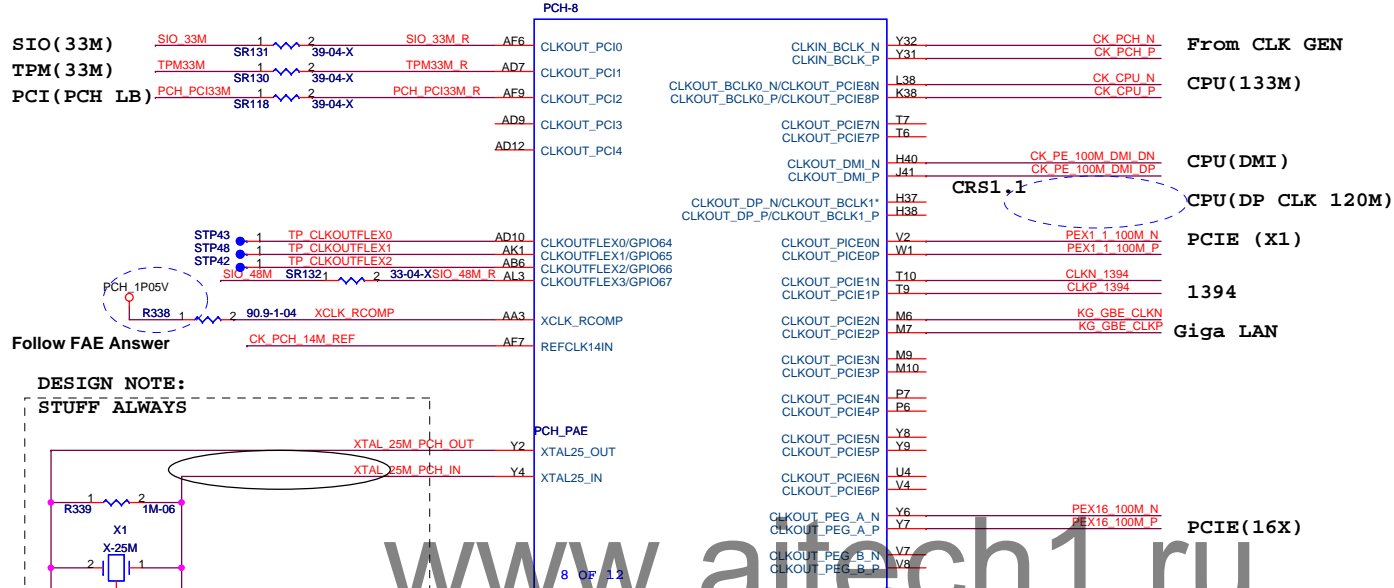
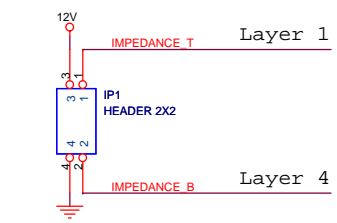
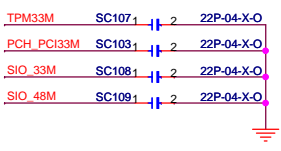
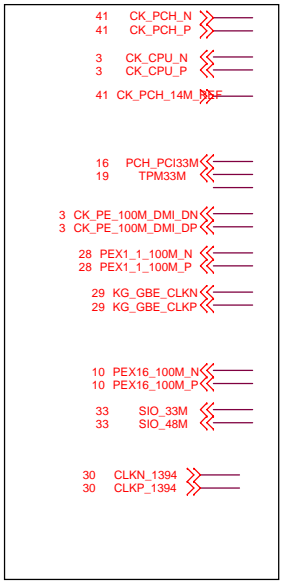




(WW07 DVI-I ONLY PORT B)

Port B: Capable of SDVO/HDMI/DVI/DP
Port C: Capable of HDMI/DVI/DP
Port D: Capable of HDMI/DVI/DP



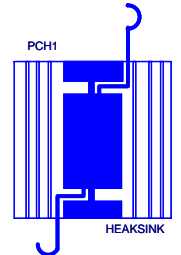


Follow FAE Answer

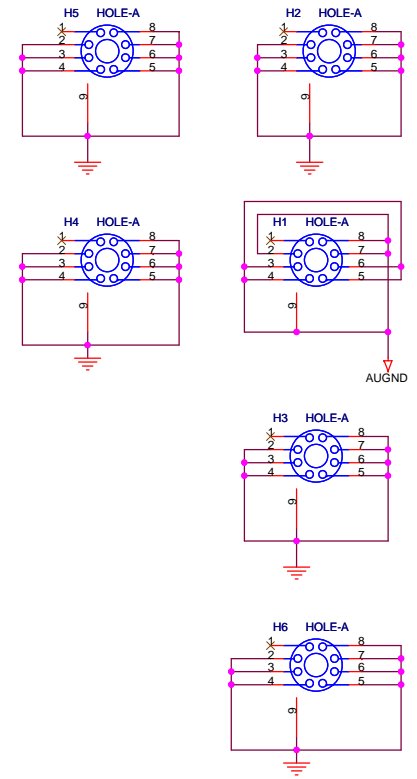
DESIGN NOTE:
STUFF ALWAYS

DESIGN NOTE:
R128 DAMPING RESISTOR
DO NOT CHANGE TO 0402

Crystal Spec: +/- 30ppm, CL=20pF
Ce=2*CL (Cs+Ci)

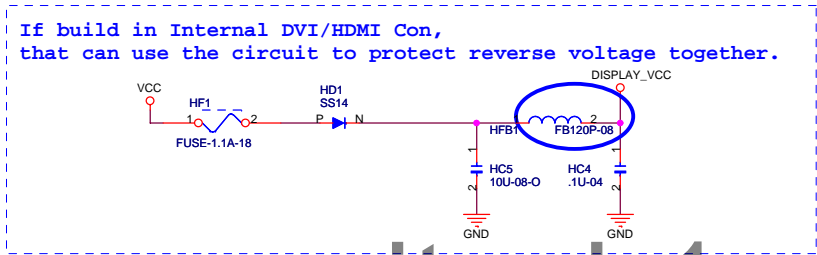
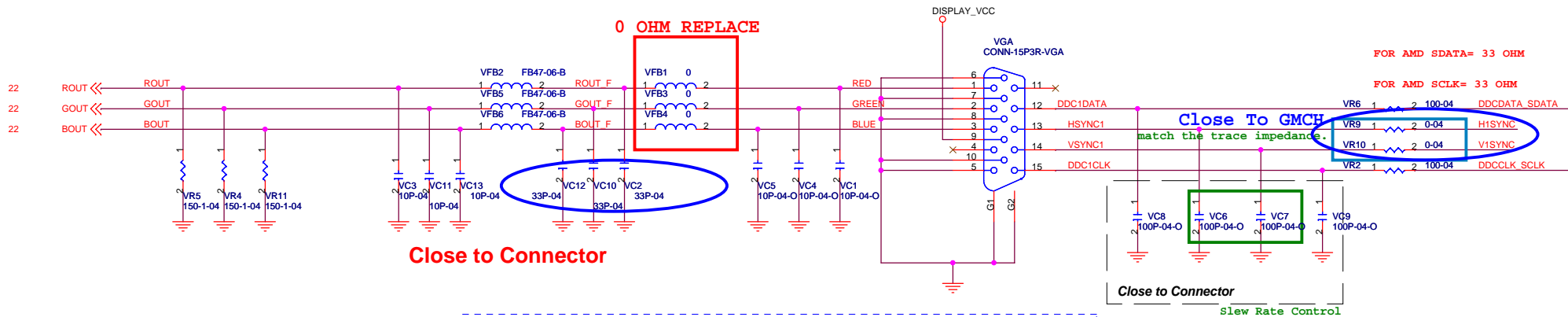


Main Part:20-120-014500

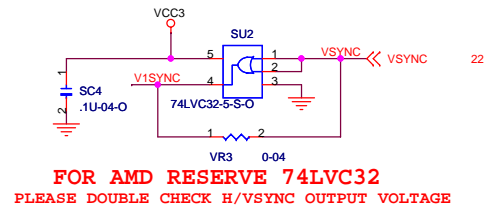
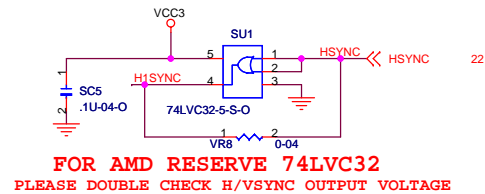
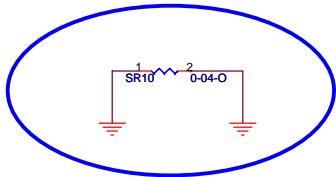
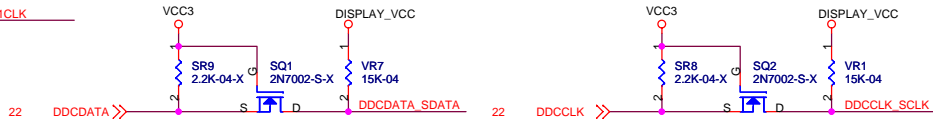
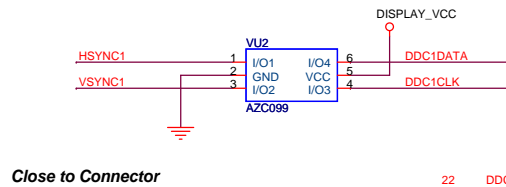
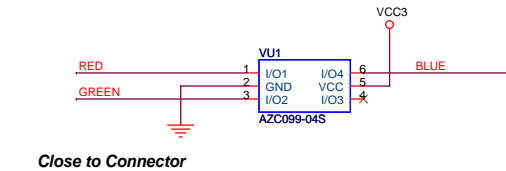


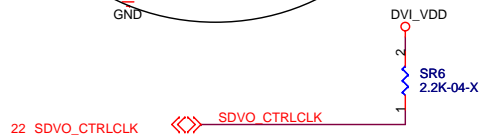
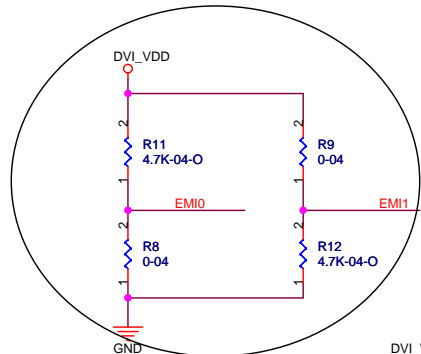
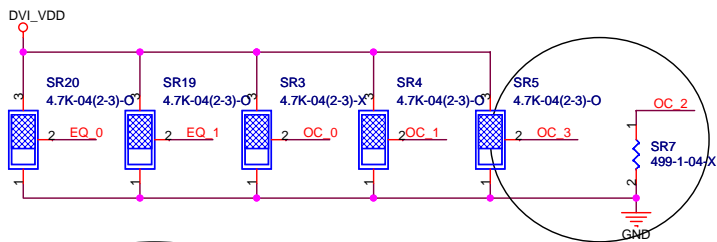
1080 : trace width 4 mil 50 ohm
Trace Length 3150 mils
Spacing: 1.clearance to itself 50/4/50(S:W:S)
2.clearance to other signal 3W

VGA Connector

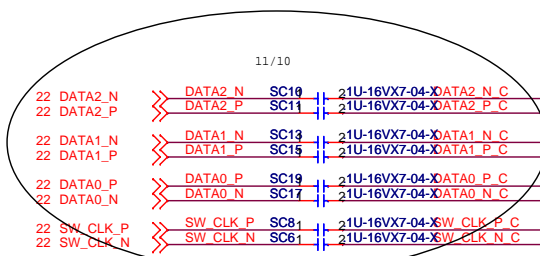
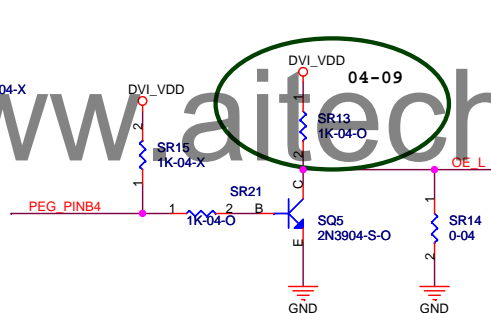


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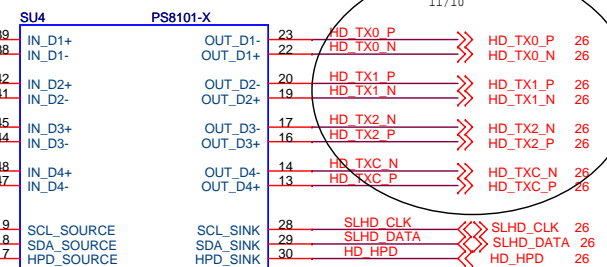


	PS8101	PI3VDP411LSTZDES
EQ_0	RESERVE 4.7K PULL UP	RESERVE 4.7K PULL DOWN
EQ_1	RESERVE 4.7K PULL UP	RESERVE 4.7K PULL DOWN
OC_0	4.7K PULL UP	RESERVE 4.7K PULL DOWN
OC_1	RESERVE 4.7K PULL UP	RESERVE 4.7K PULL DOWN
OC_2	499 1% OHM PULL DOWN	RESERVE 4.7K PULL DOWN
OC_3	NC	RESERVE 4.7K PULL DOWN
PEG_PINB4	RESERVE 4.7K PULL UP	NC
HR20	NC	20K-04

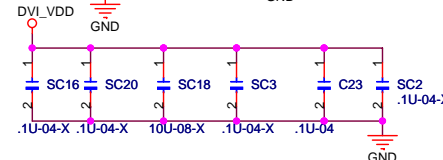
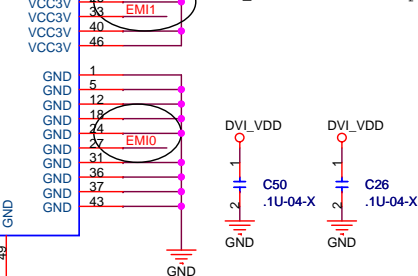


DDC_EN	Passgate
3.3V	Enable
0	Disable

Level Shifter



HD_TX0_P	HD_TX0_N	HD_TX1_P	HD_TX1_N	HD_TX2_P	HD_TX2_N	HD_TXC_P	HD_TXC_N
26	26	26	26	26	26	26	26

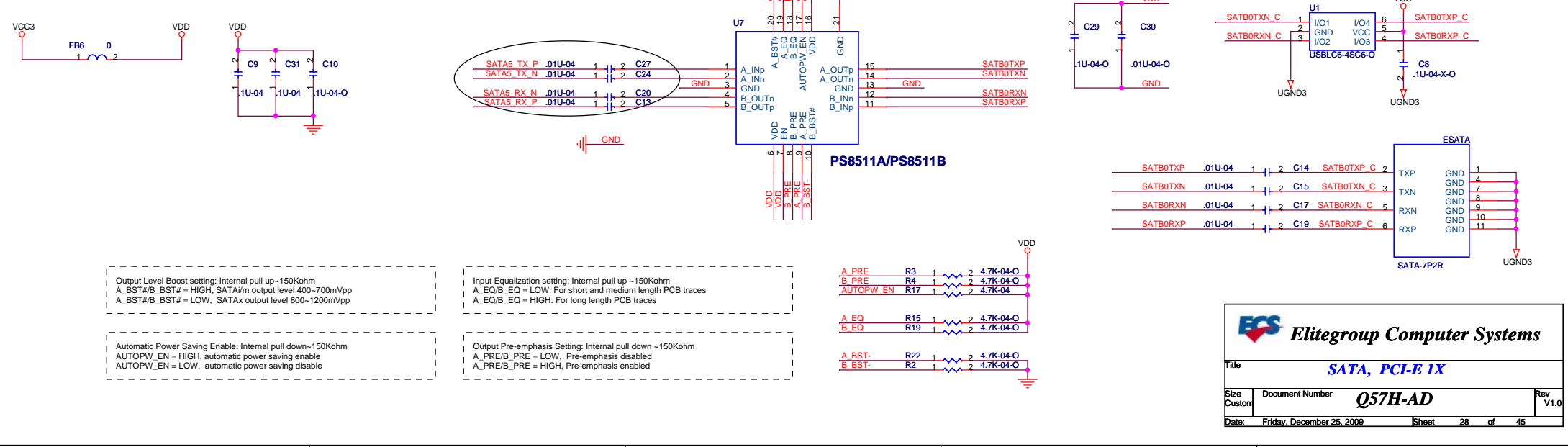
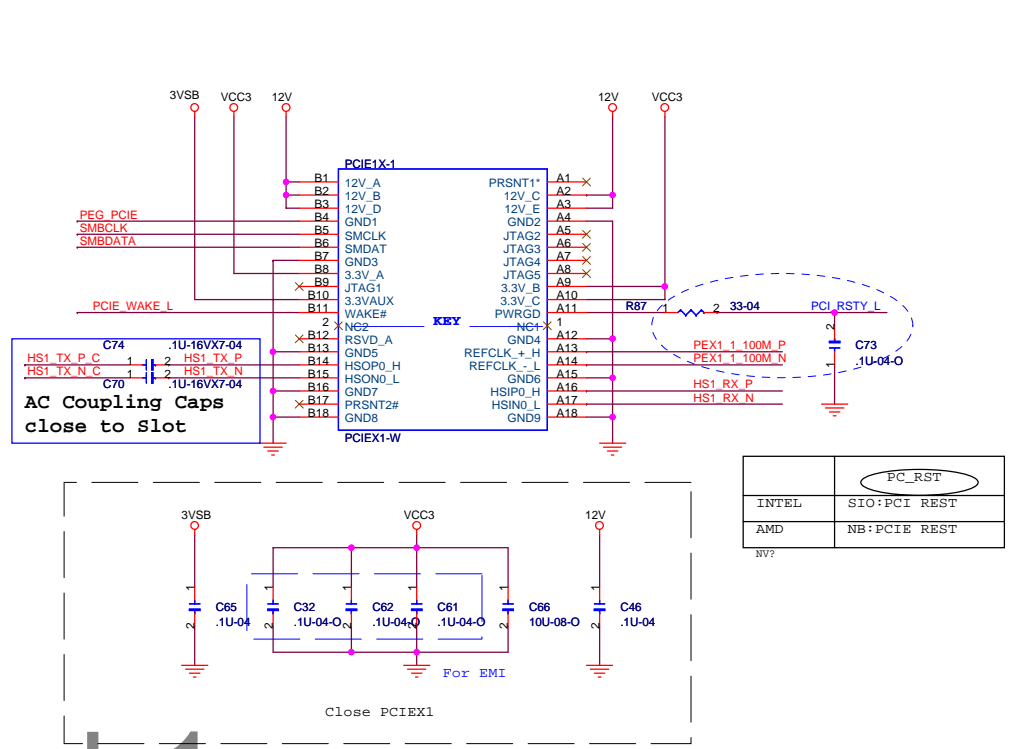
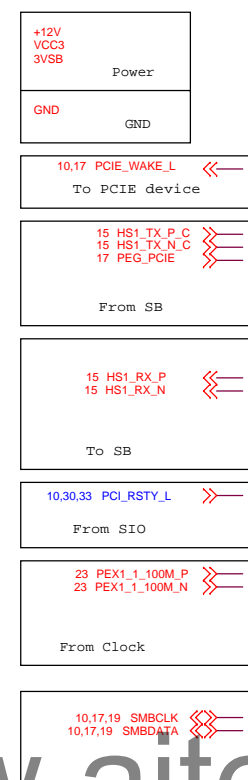
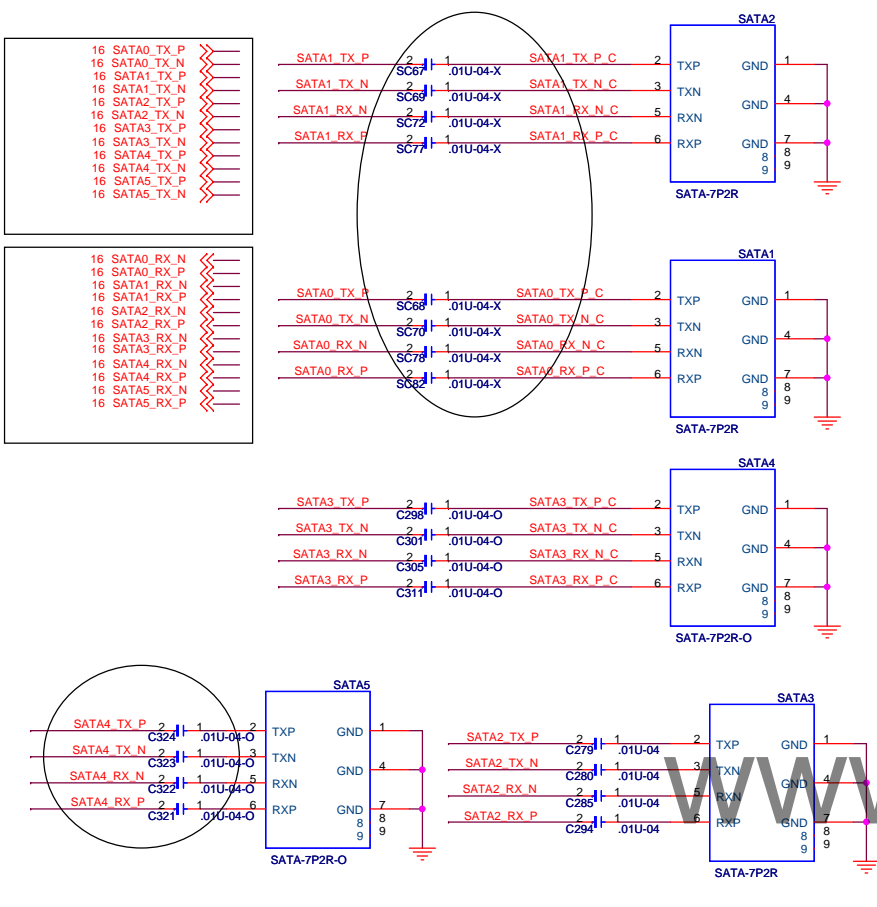


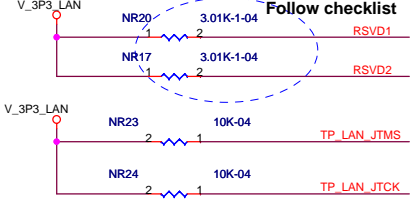
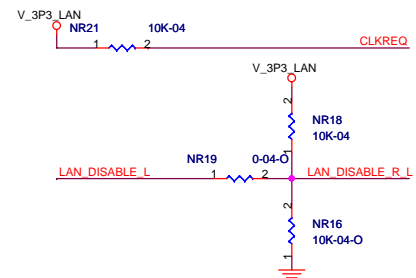
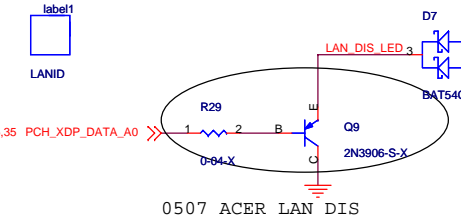
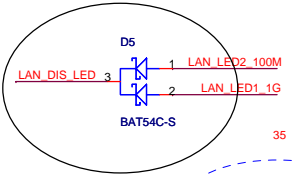
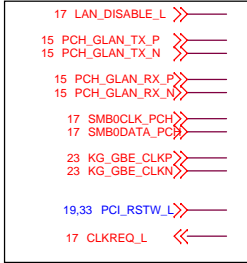
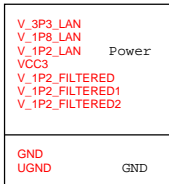
FOR PS8101			FOR PI3VDP411LSTZDES		
OC_3	OC_2	OC_1	OC_0	Vswing(mV)	Pre/De-emphasis
0	0	0	0	500	0
0	0	0	1	600	0
0	0	1	0	750	0
1	1	1	1		



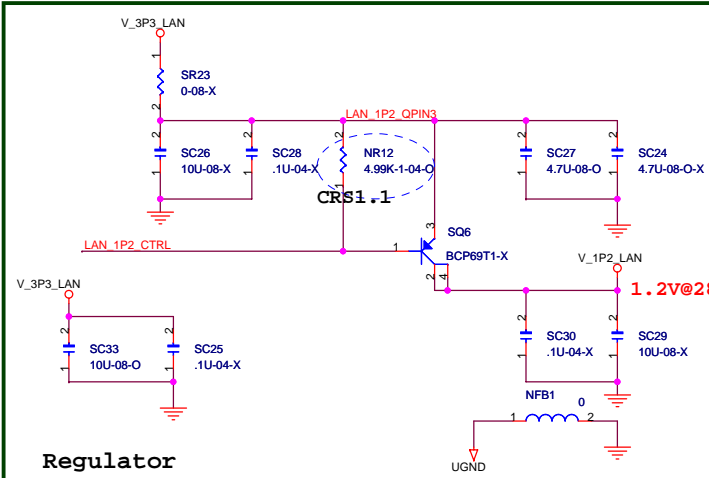
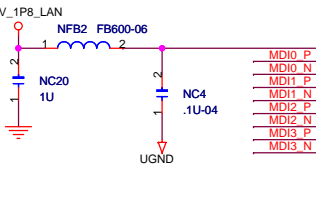
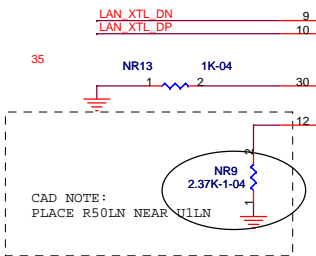
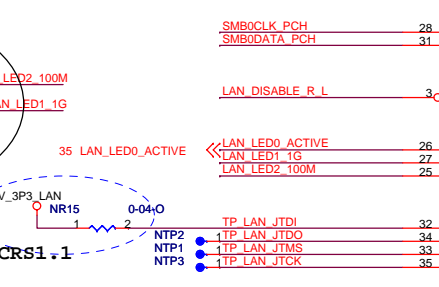
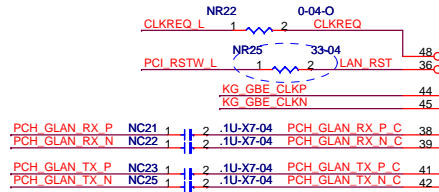
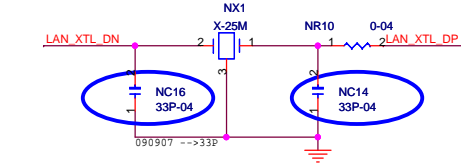
Elitegroup Computer Systems

Title	HDMI Interface (Switch, Level shifter)		
Size	Document Number	Q57H-AD	
Custom			
Date:	Friday, December 25, 2009	Sheet	25 of 45

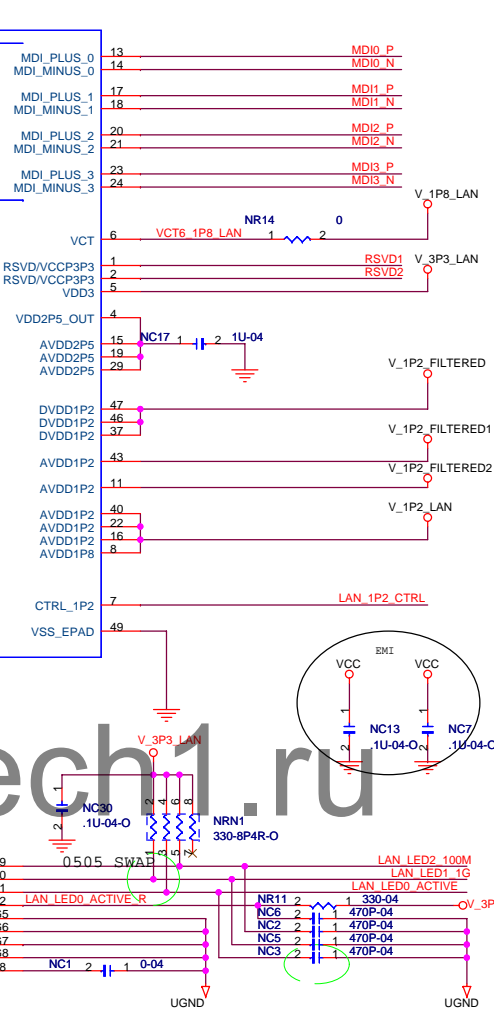
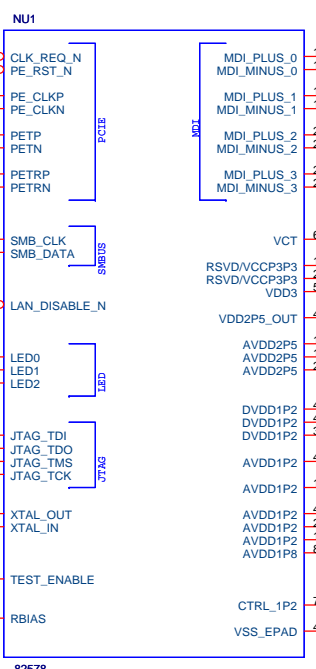




Crystal Spec: $\pm 30\text{ppm}$, $CL=20\text{pF}$
 $Ce=2*CL - (Cs+Ci)$

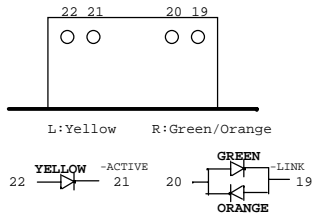
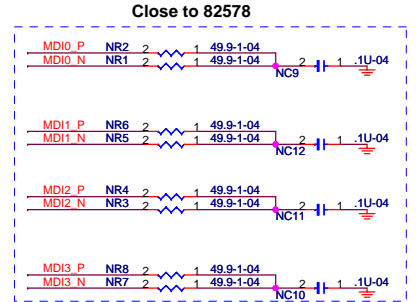
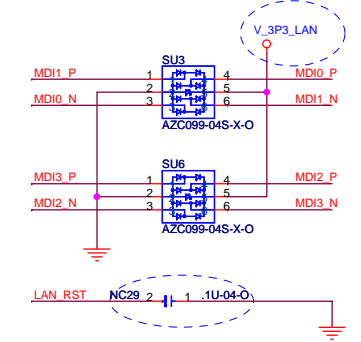


Regulator



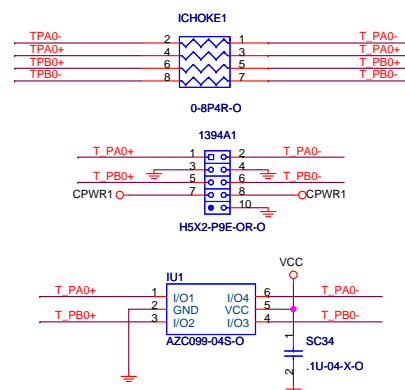
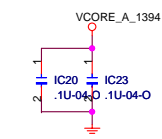
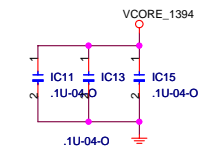
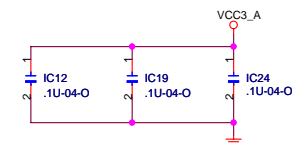
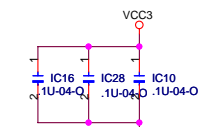
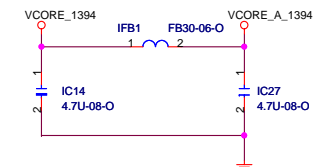
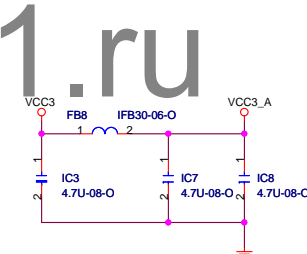
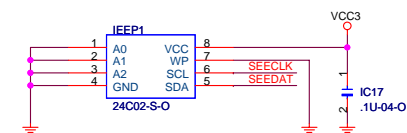
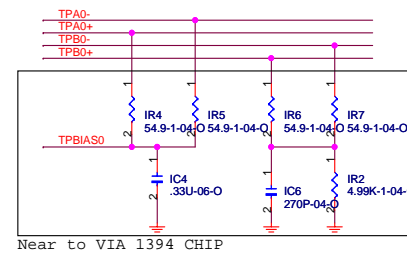
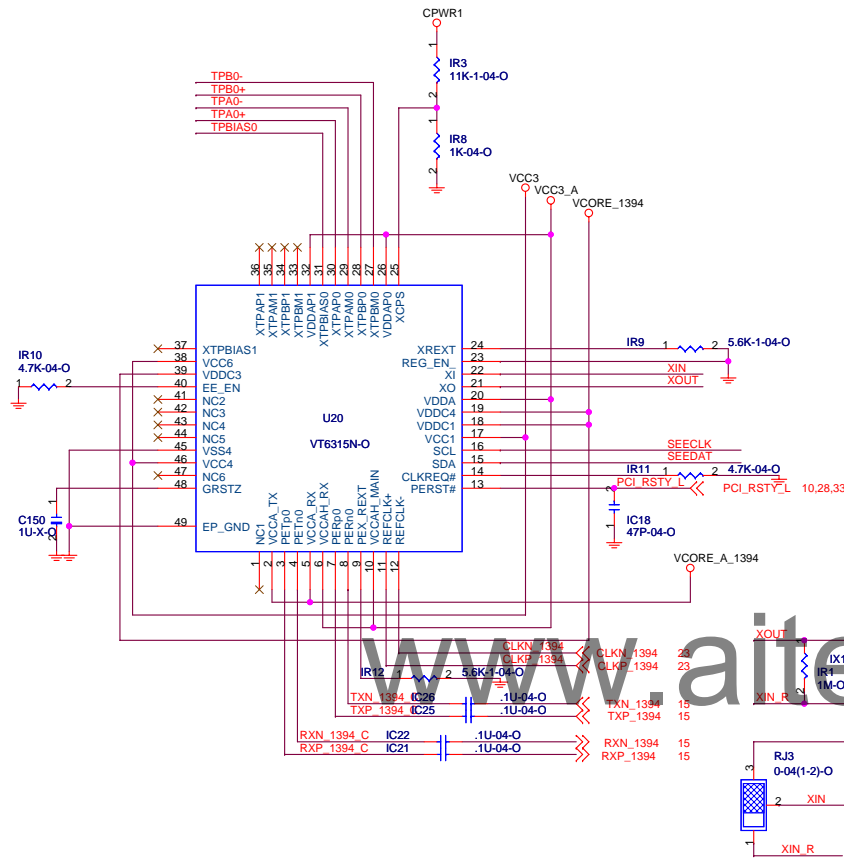
WOL	Status	Yellow	Gre/Ora
Don't Care	No link	OFF	OFF
OFF	S3/S4/S5	OFF	OFF
ON	10M,Inactive	OFF	OFF
ON	10M,Active	YB	OFF
ON	100M/Inactive	OFF	G
ON	100M/Active	YB	G
ON	1G,Inactive	OFF	O
ON	1G/Active	YB	O

Remark: Y/G/O-->Color, B-->Blinking

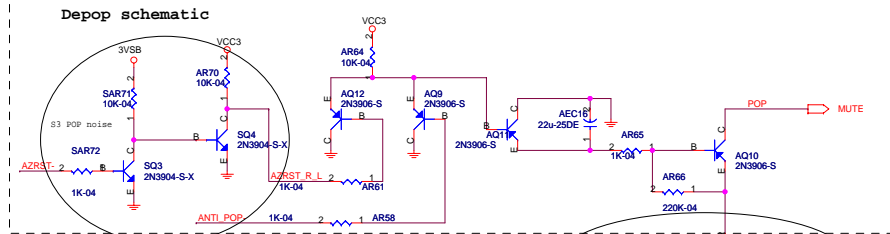


1.8V@465mA (181+284)

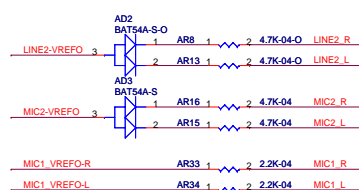
shadow EEPROM	ON	OFF
R215	V	X



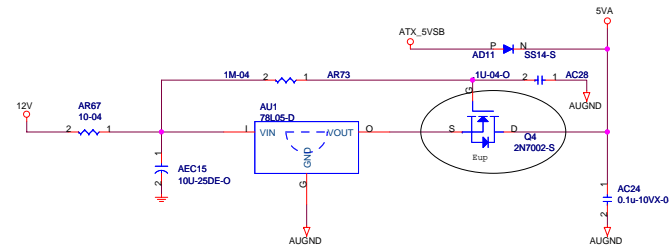
Depop schematic



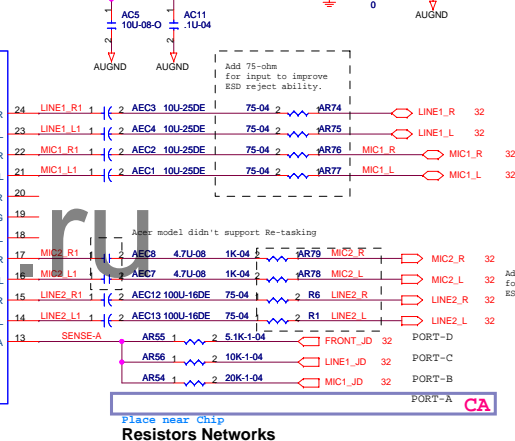
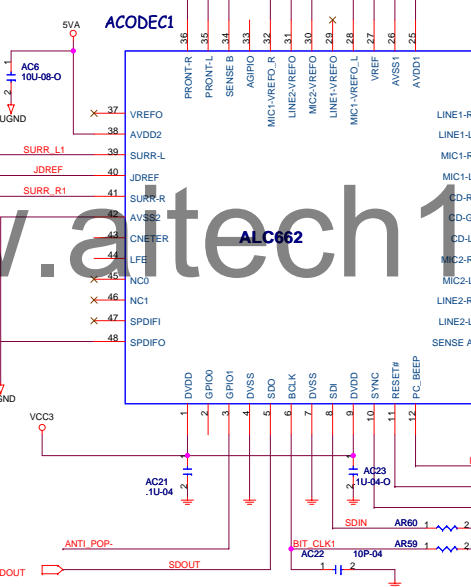
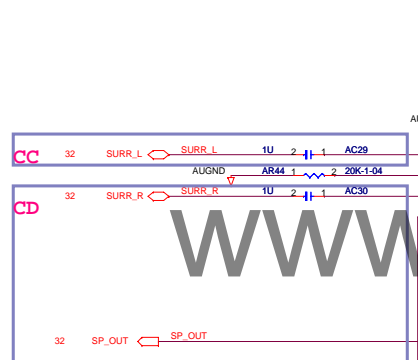
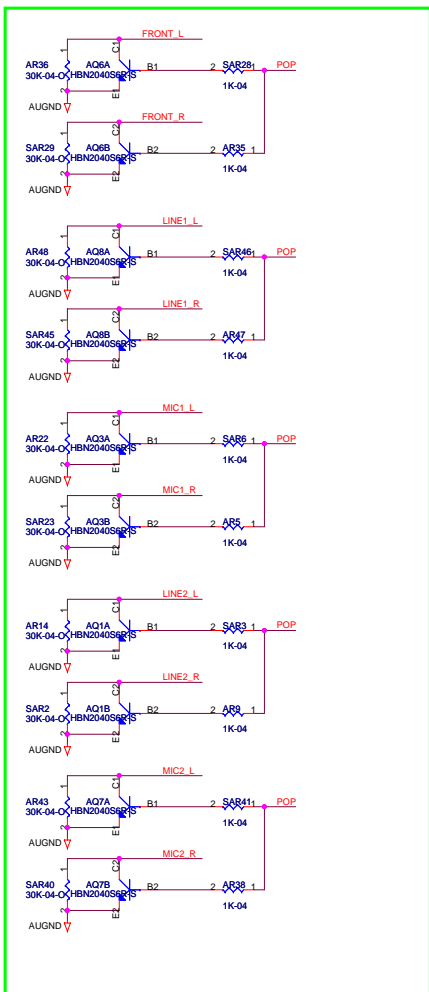
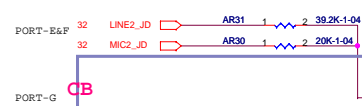
MIC Bias



Improve the background noise of MIC boost



Place near Chip Resistors Networks

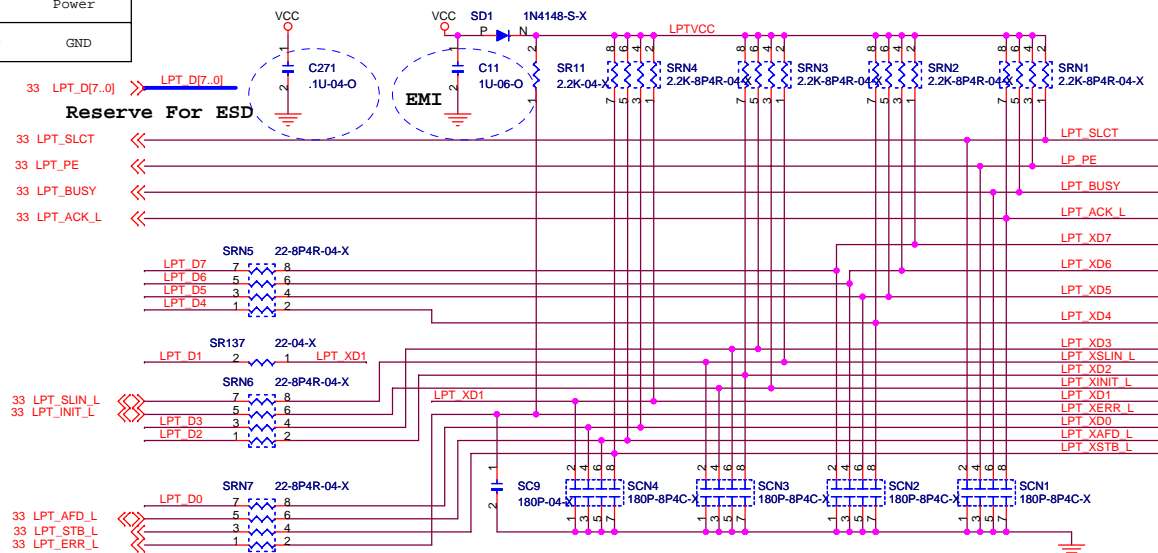


ALC662 IO Difference

Location	ALC662 3+2PORT	ALC888S 5+2PORT (Default)
CA	X	V
CB	X	V
CC	X	V
CD	X	V
CE	X	V
CF	X	V
CG	AUDIO-3P-HDA	AUDIO-25P-SPE
CH	V	X
CI	X	X
CJ	X	V

VCC	Power
GND	GND

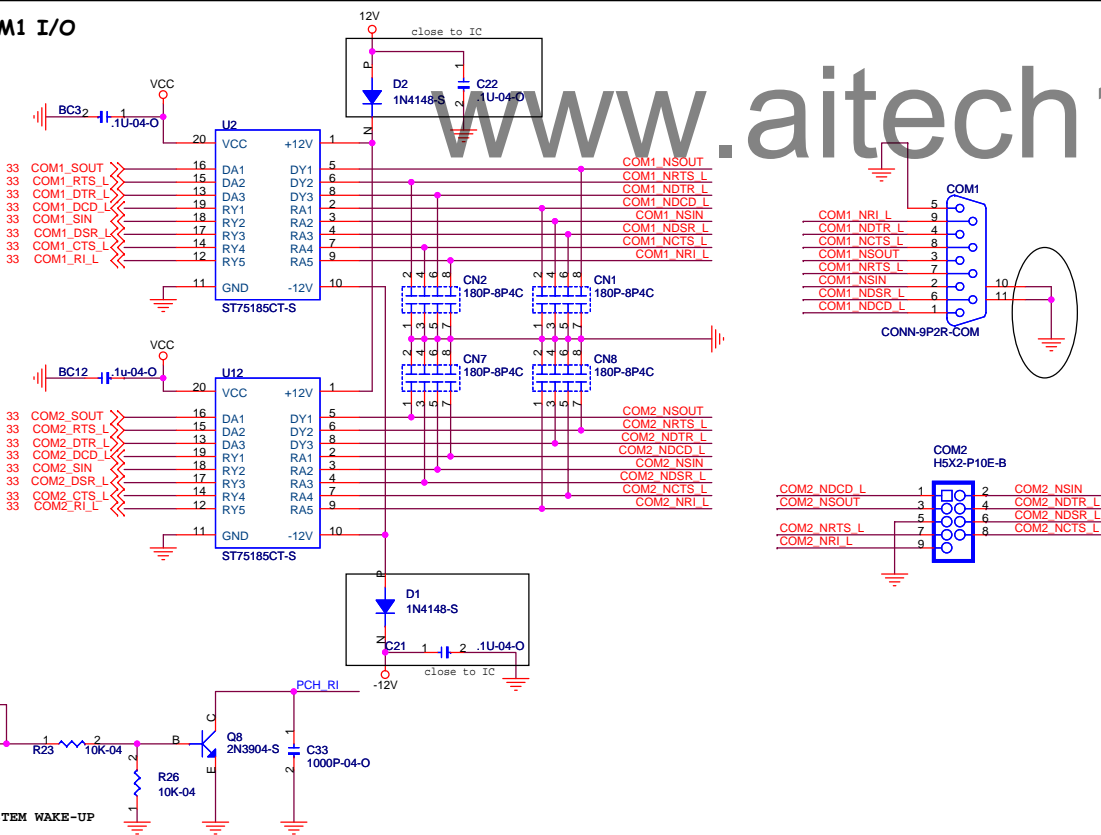
LPT



+12V	Power
-12V	GND
VCC	GND

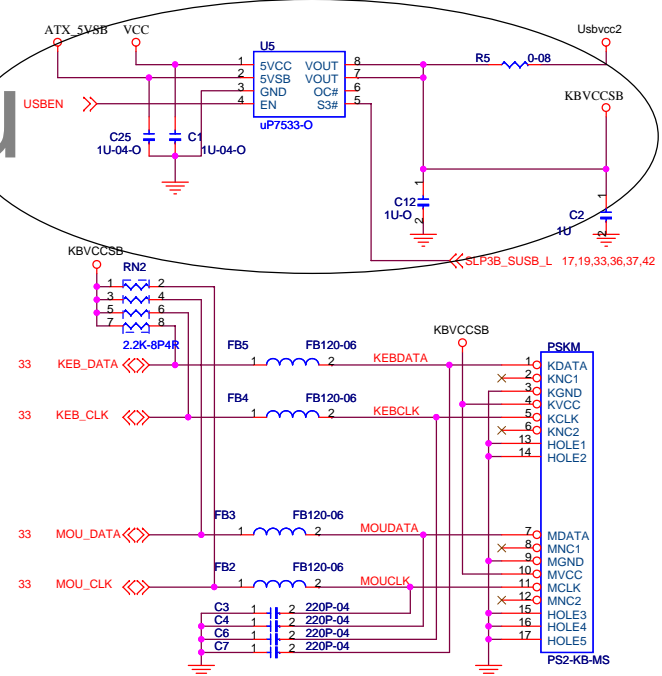
COM1 I/O

17 PCH_RI	TO SB
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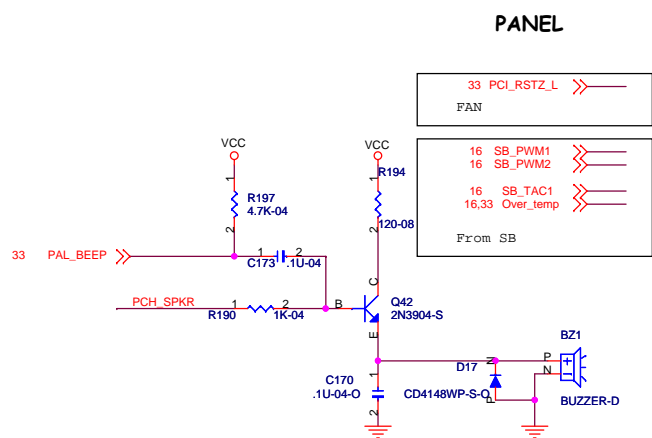
KEYBOARD & MOUSE

USB1 5VDUAL	Power
KBVCCSB	GND
GND	GND



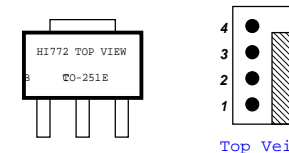
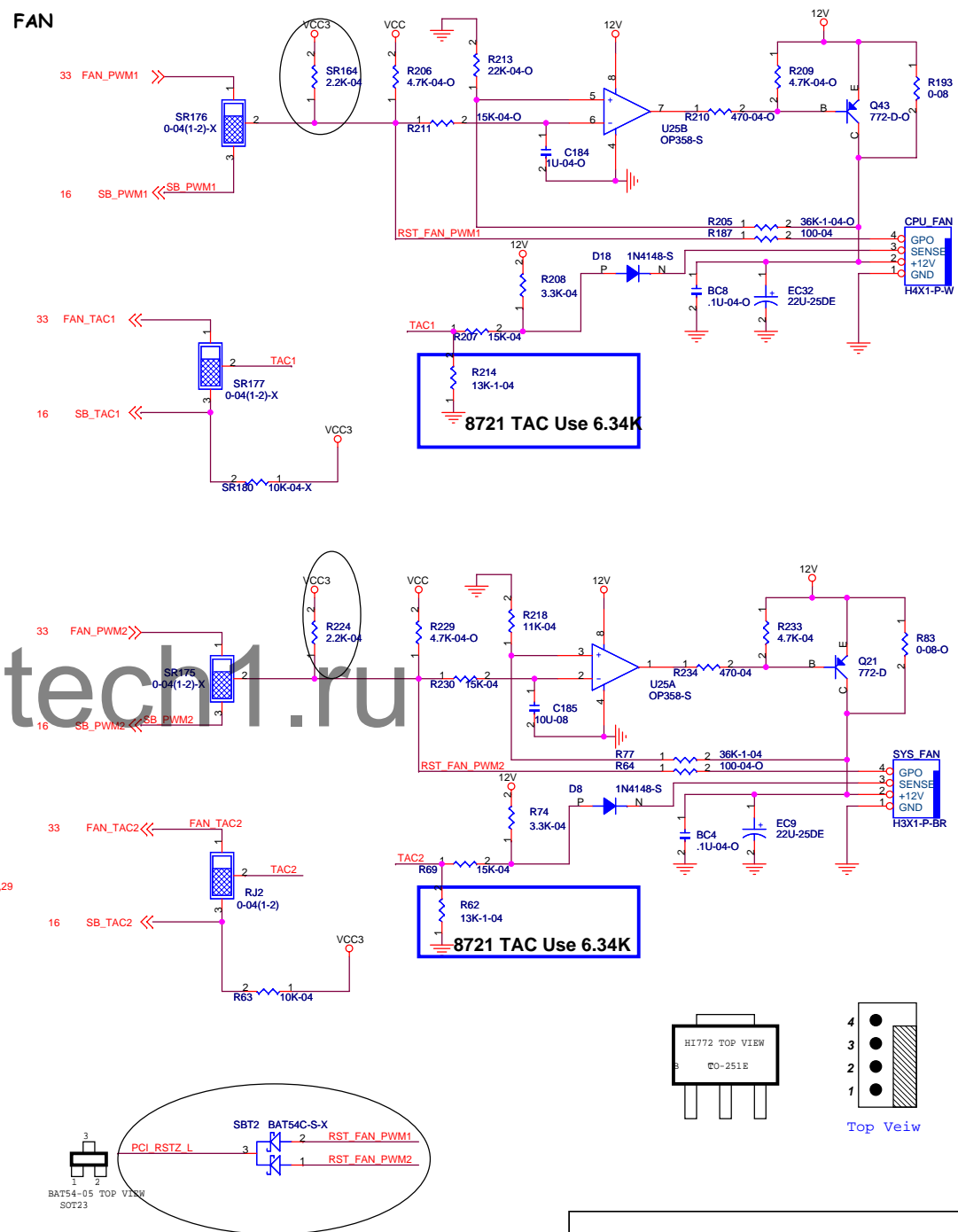
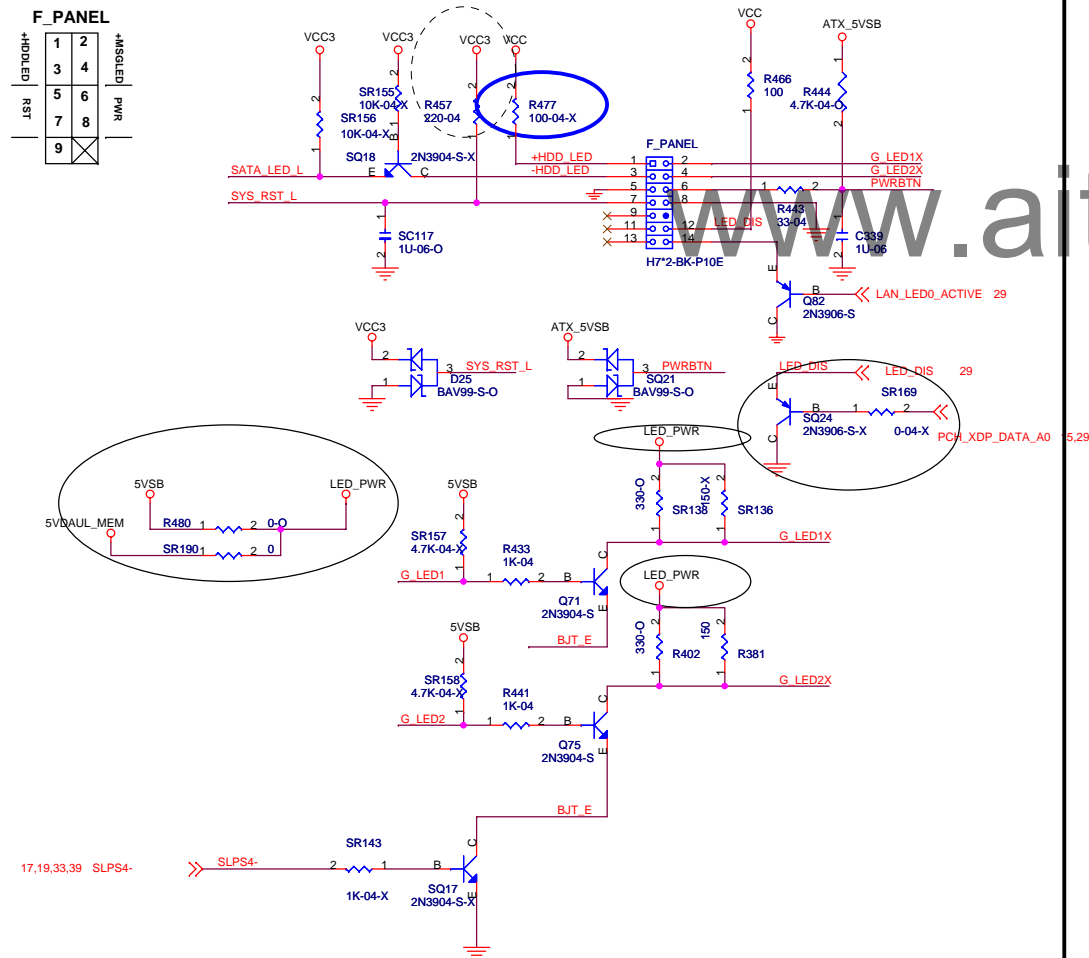
Elitegroup Computer Systems

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Size	Document Number
Custom	Q57H-AD
Date	Friday, December 25, 2009
Sheet	34 of 45
Rev	V1.0

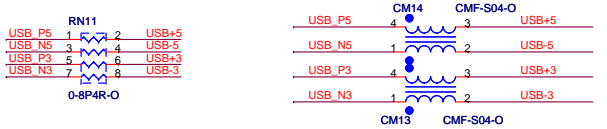
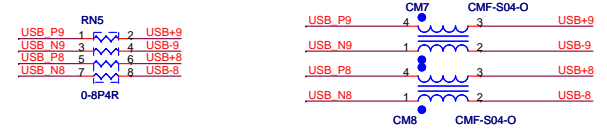
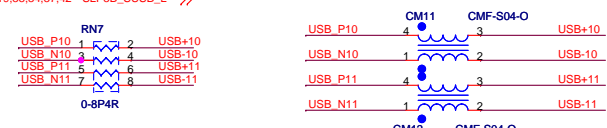


	S0	S1	S3	S4	S5
G_LED1	L	B	B	L	L
G_LED2	H	H	L	L	L
Status	G	GB	YB	OFF	OFF
Remark	B:Blinking				

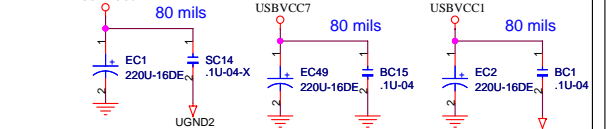
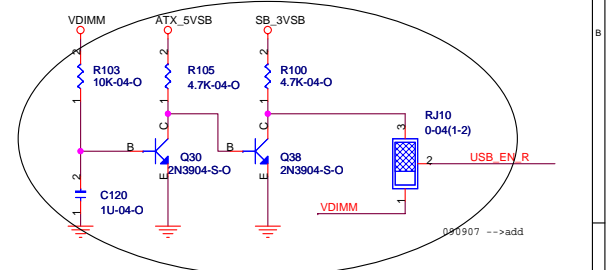
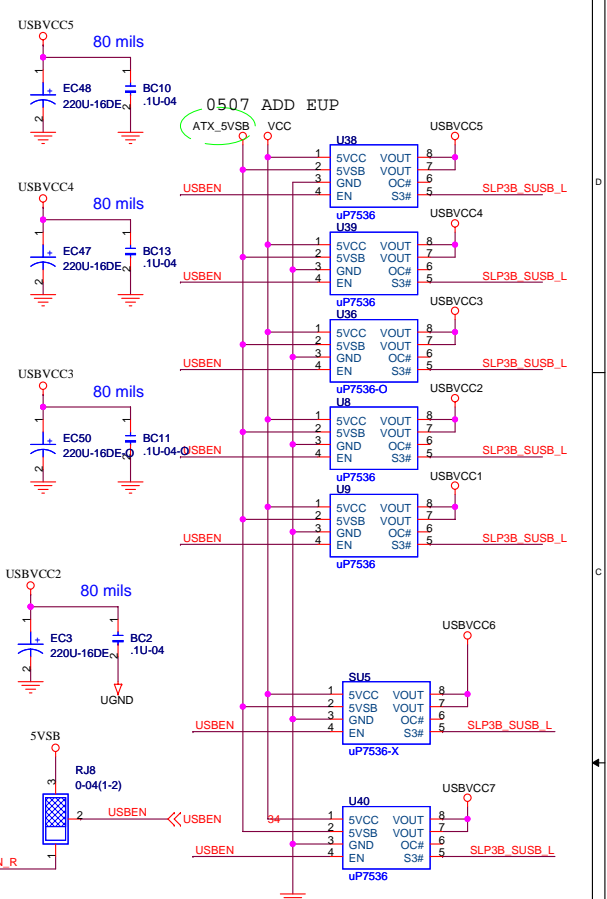
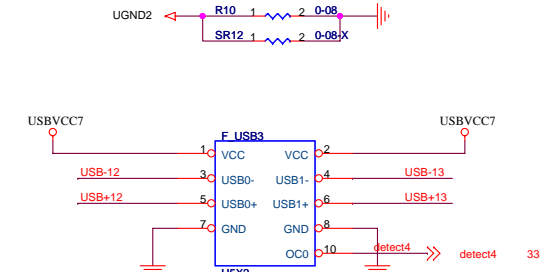
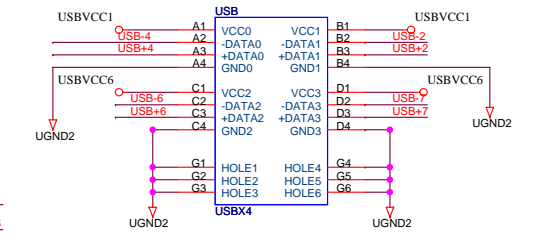
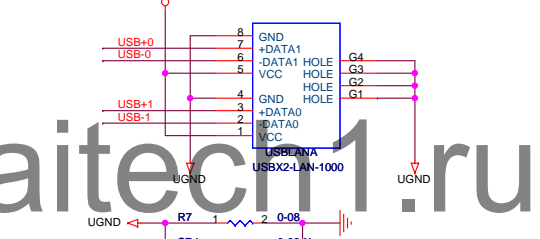
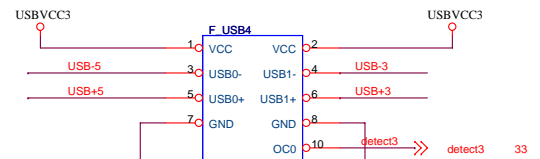
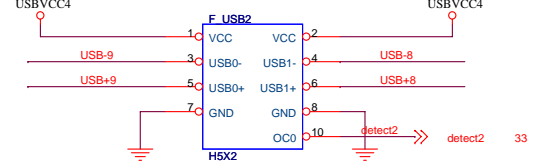
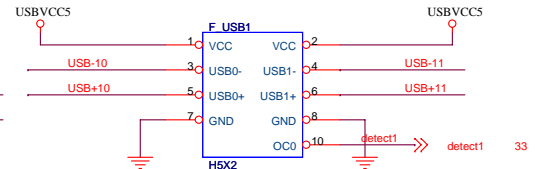
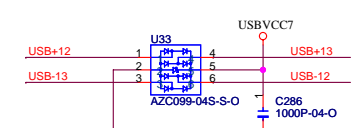
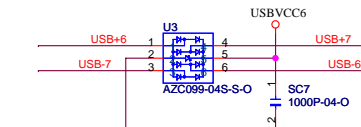
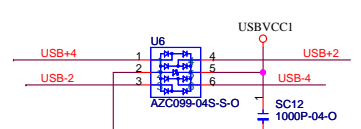
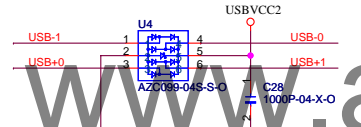
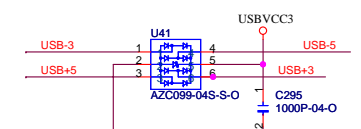
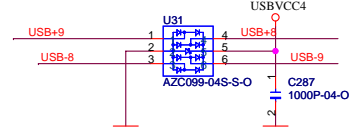
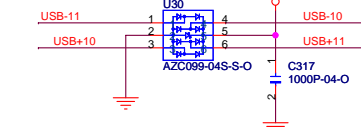
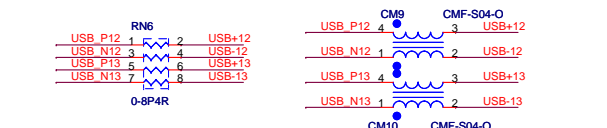
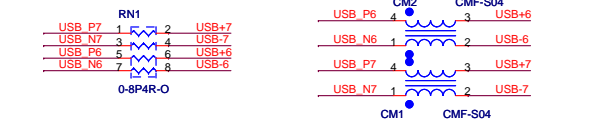
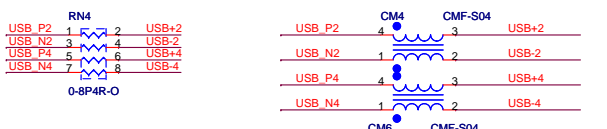
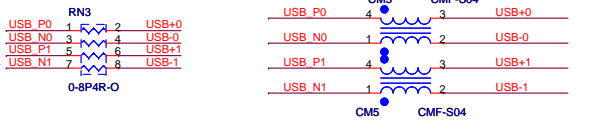
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090119
WW51 SYS_RST_L should
pull high to VCC3 not 3VSB and 220 ohm
```

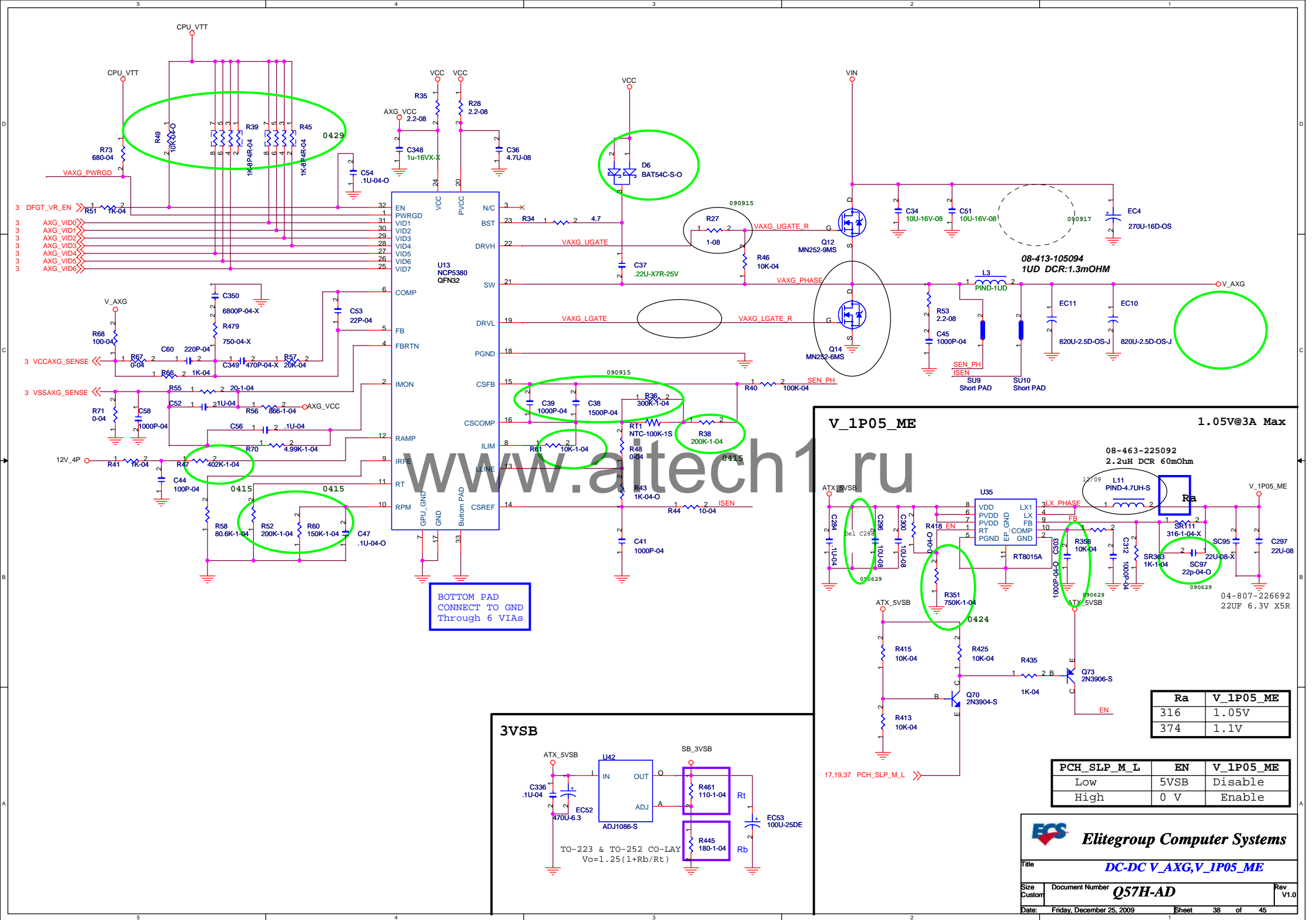


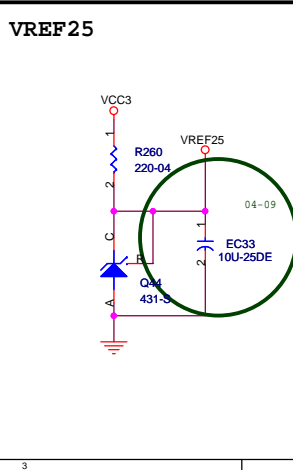
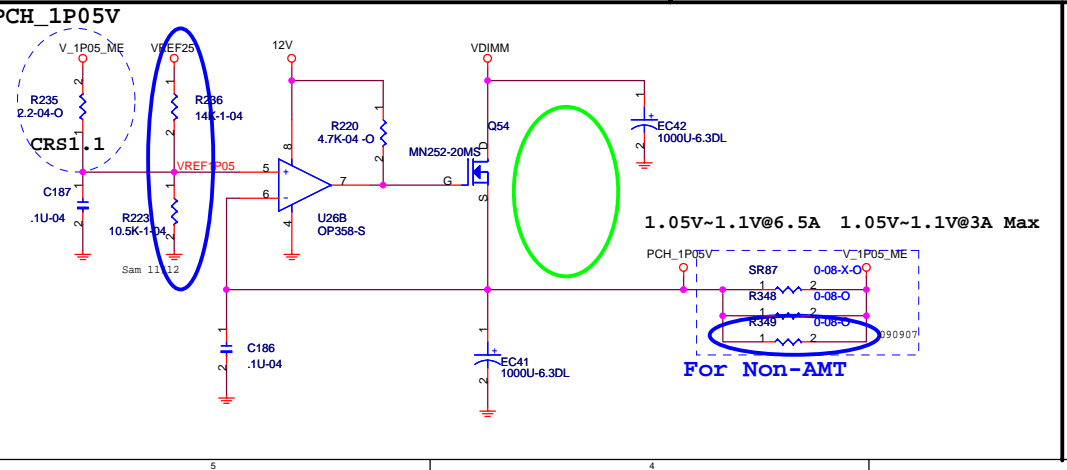
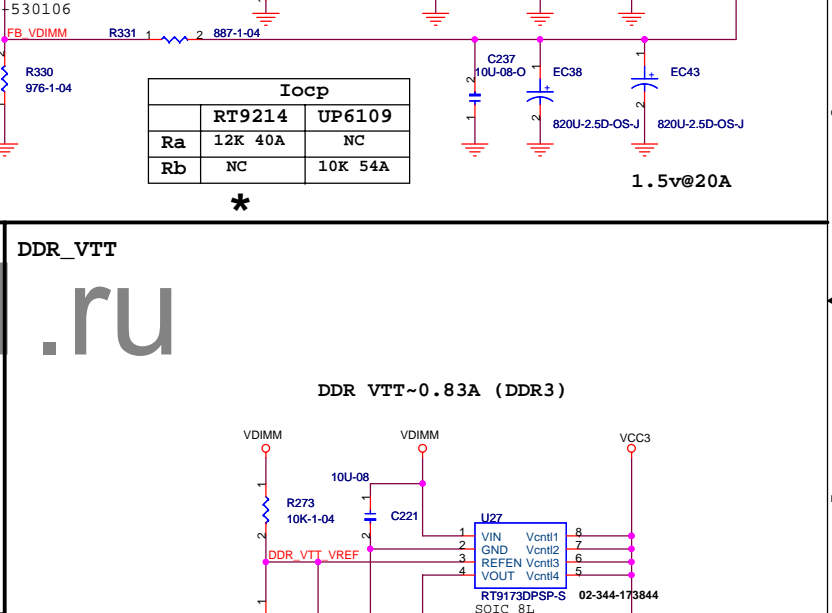
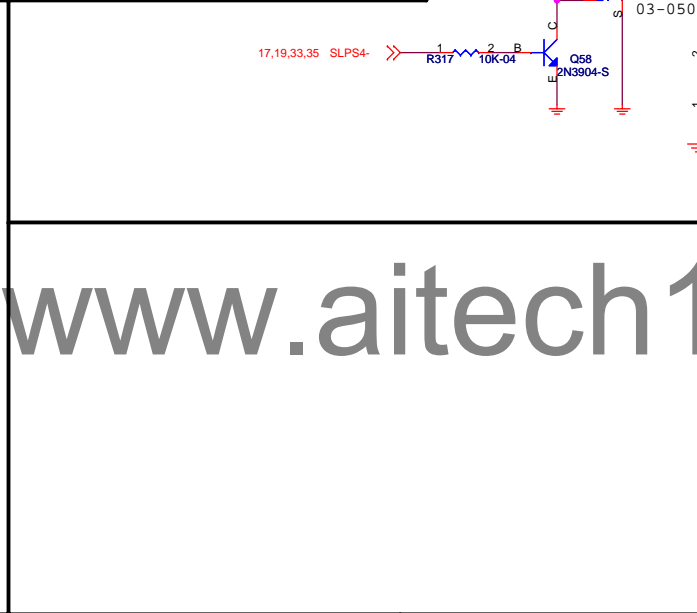
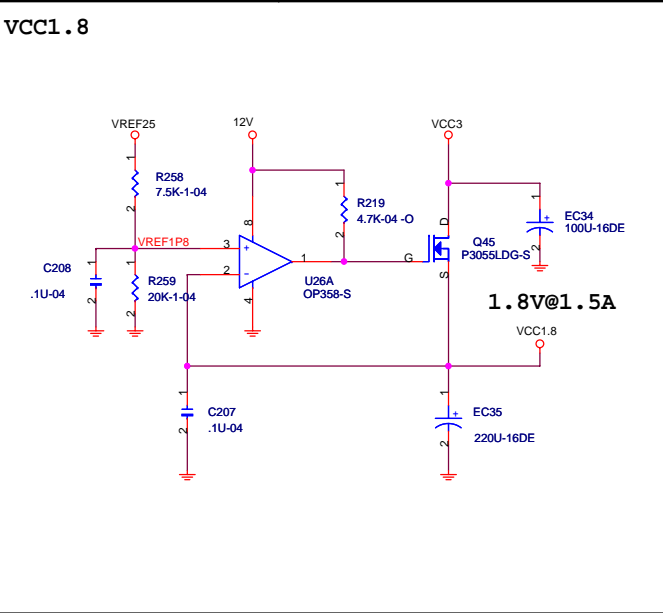
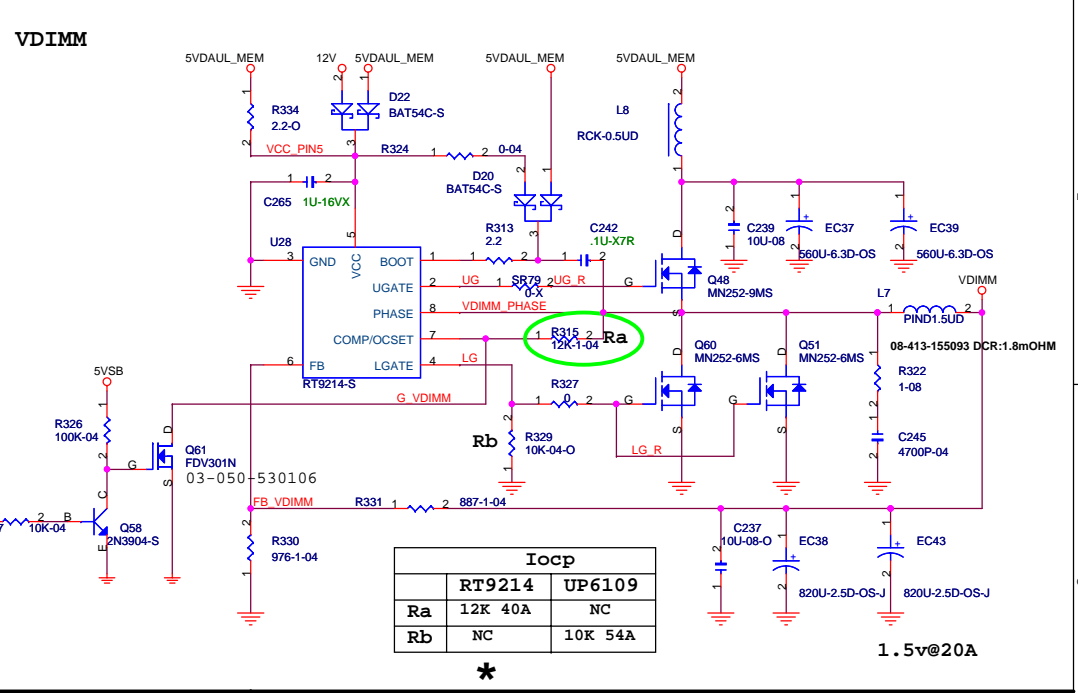
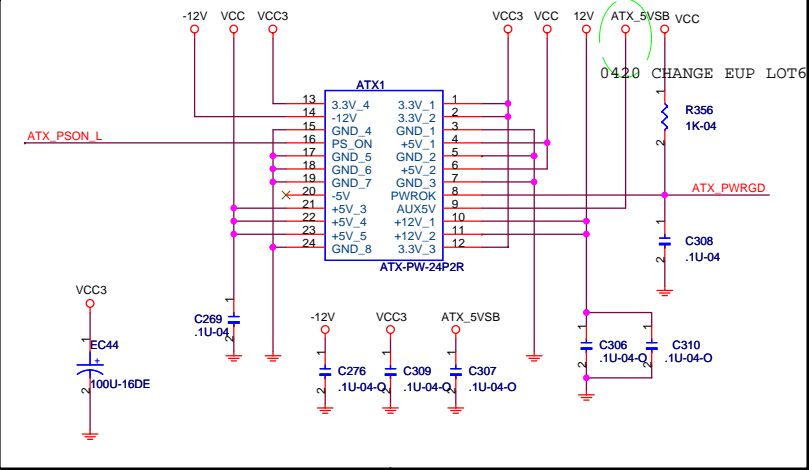
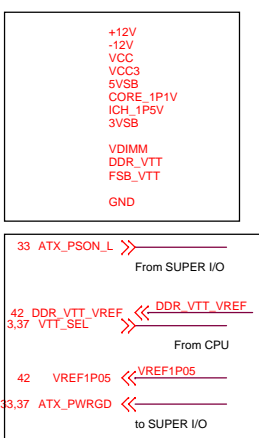
15 USB_P[13..0] >> USB_P[13..0]
 15 USB_N[13..0] >> USB_N[13..0]
 17,19,33,34,37,42 SLP3B_SUSB_L >> SLP3B_SUSB_L



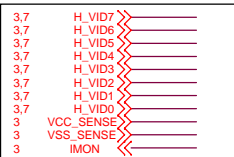
0429 CHANGE FOOTPRINT





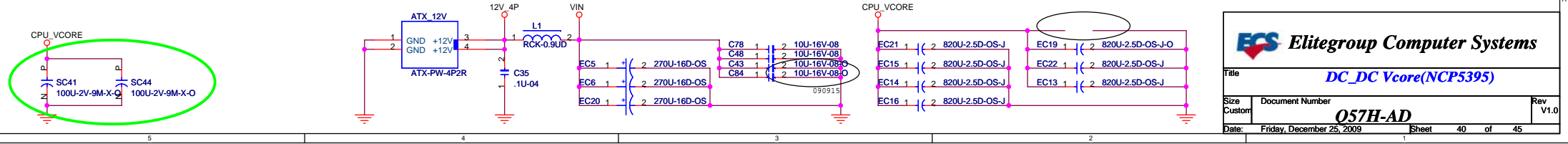
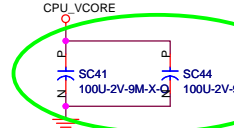
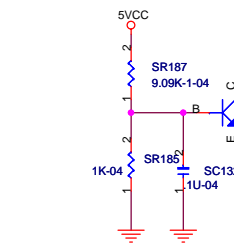


VCORE VCC CPU_VTT	POWER
GND	GND



From CPU

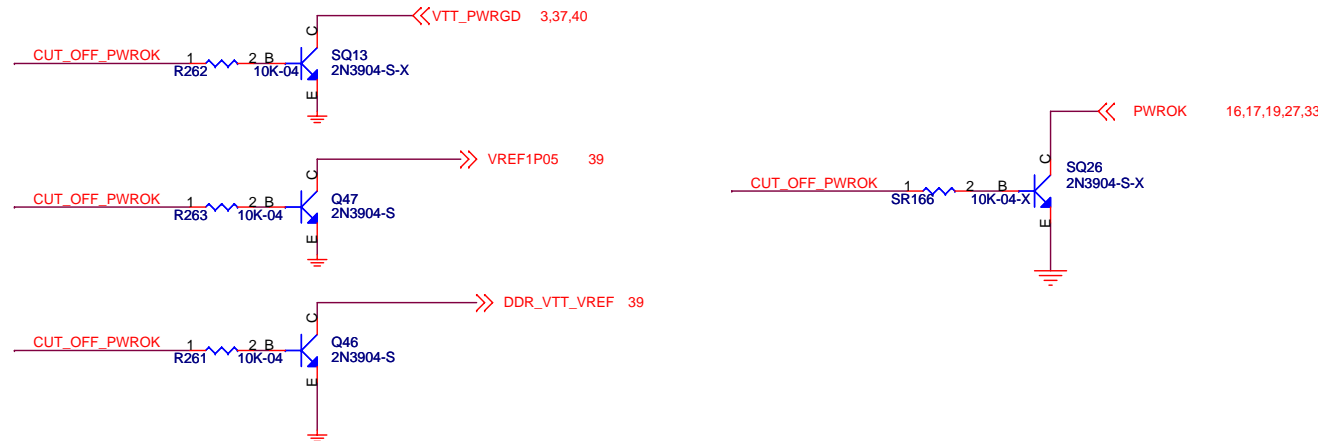
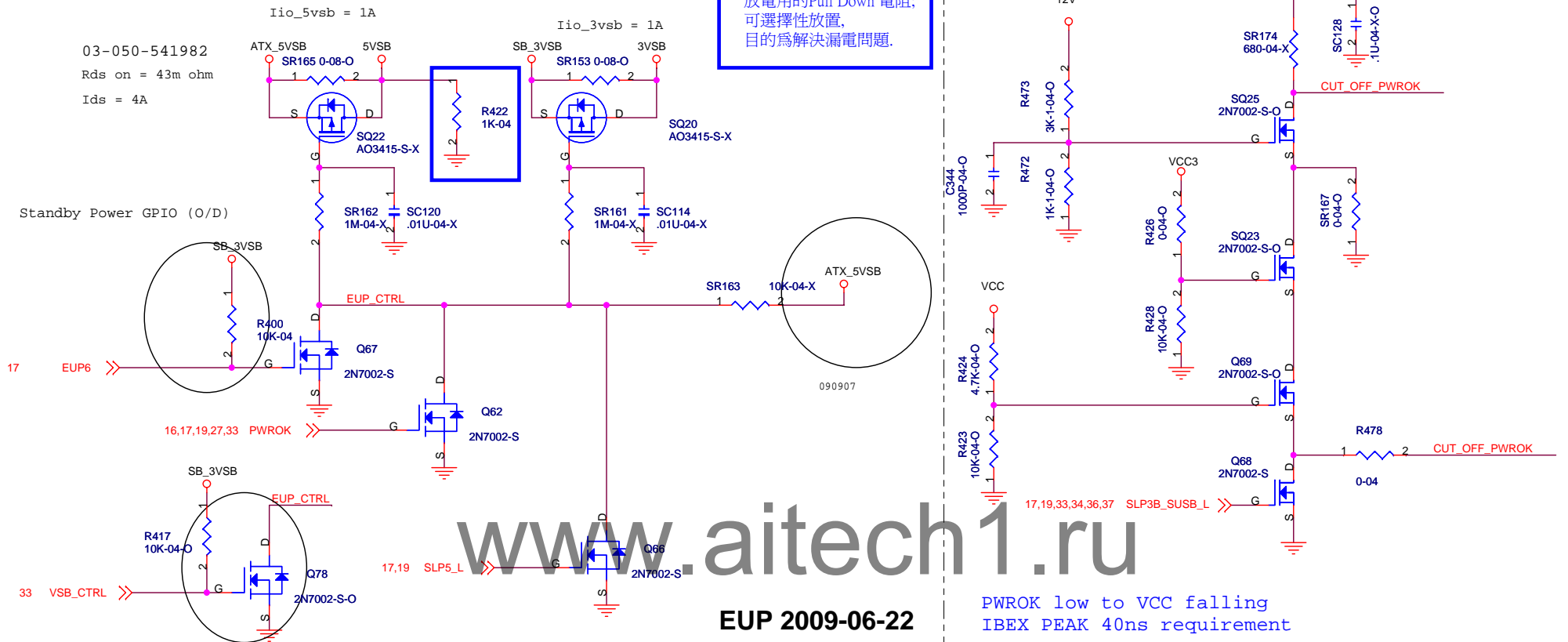
To CK505



	Ra	Rb	Ca
NCP5395	Open	0 ohm	Open
NCP5395T	10K	1K	Reserve

PS:NCP5395T is new IC for
PSI transient improvement

放電用的Pull Down 電阻;
可選擇性放置,
目的為解決漏電問題.



Elitegroup Computer Systems			
Title			
EUP LOT6			
Size	Document Number		Rev
Custom	Q57H-AD		V1.0
Date:	Friday, December 25, 2009		Sheet 42 of 45

